Double Patterning Jumps the 200wph Hurdle: Coat/Develop Track Equipment

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SOKUDO Lithography Breakfast Forum
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"Photo" Double Patterning Resist Process Options

	Litho-Freeze chemical b/w 1st & 2nd Resist	Self-Freeze by 2nd Resist Coat & Bake	UV Cure Freeze	Negative Tone Dev. Resist	Evaluation Partners per Technical Papers
JSR	☻	○	△	--	IMEC, Albany
TOK	--	☻	--	--	Nikon, IMEC
FujiFilm	--	--	--	☻	IMEC
Rohm & Haas	○	○	--	--	CEA-LETI
Shin-Etsu	--	○	△	--	AMD, Ushio, Sokudo/ AMAT

Possible with SOKUDO DUO

Litho-Freeze: Complex Process on Track but Good Results !!!

Self-Freeze: Preferred but Weak Results (will improve)

UV Cure Freeze: Needs More R&D Effort but Attractive if it can work!

Negative Tone Dev. Resist: Potential for Niche Apps. (trench, CH)

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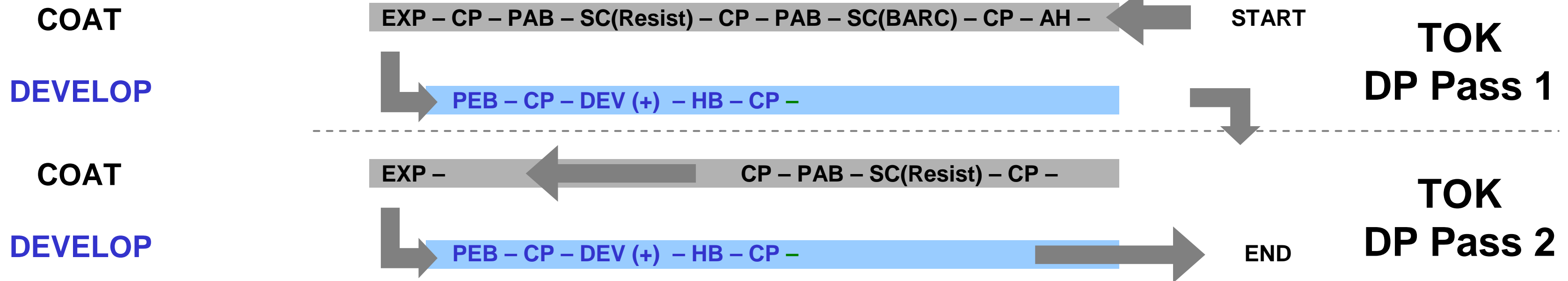
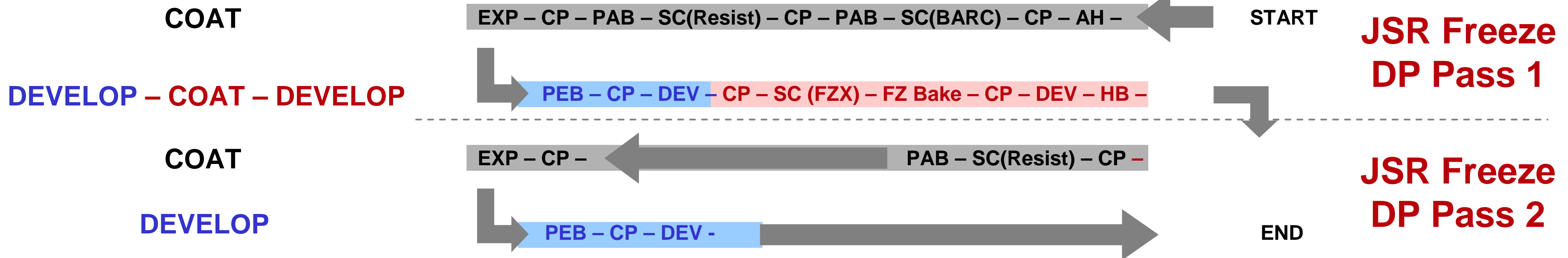
"Photo" Double Patterning Resist Process Example

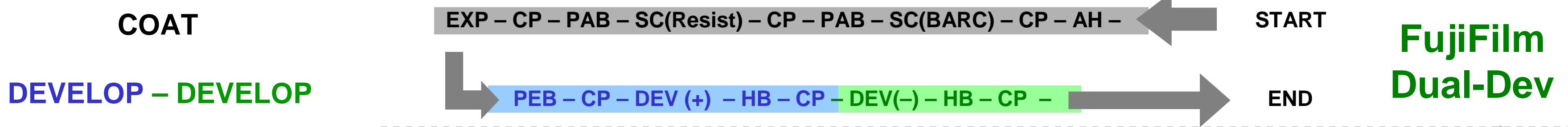
TOK Freeze-Free



JSR Freeze-Coat

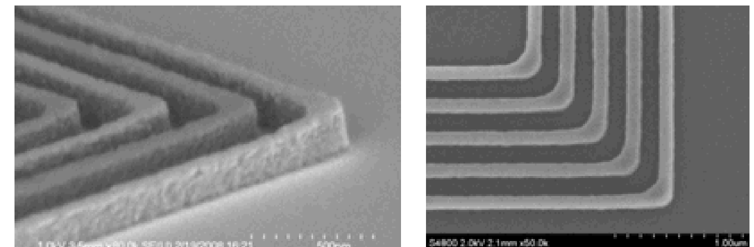


FujiFilm Dual-Develop



Myth: Semiconductor IC manufacturers only need one Double Patterning Solution that works for them

- **Reality: One Double Patterning Solution will not cover all IC process pattern scenarios, will need multiple "photo" Double Patterning solutions:**
  - Dense lines (straight)
  - Dense lines (elbow)
  - Contact holes, dense / iso
  - Trench patterns
  - Etc.



- **Therefore… Coat/Develop Track needs flexibility to run whatever "Double Patterning Solution" that fits the IC process pattern layer**

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>200wph Double Patterning
Requirements for Coat/Develop Track

- **Flexibility to run <u>whatever</u> "Double Patterning Solution" that fits the IC process pattern layer**
  - Coat/develop track should not limit options of manufacturer
- **Maintain >200wph throughput even with extra process steps demanded by each Double Patterning solution**
  - Expandable to support adding coat, develop and bake units
  - Enable multi-pass flows (i.e. two-step develop in one flow)
- **Maintain continuous supply of wafers inside track: FOUP / Wafer Buffering**

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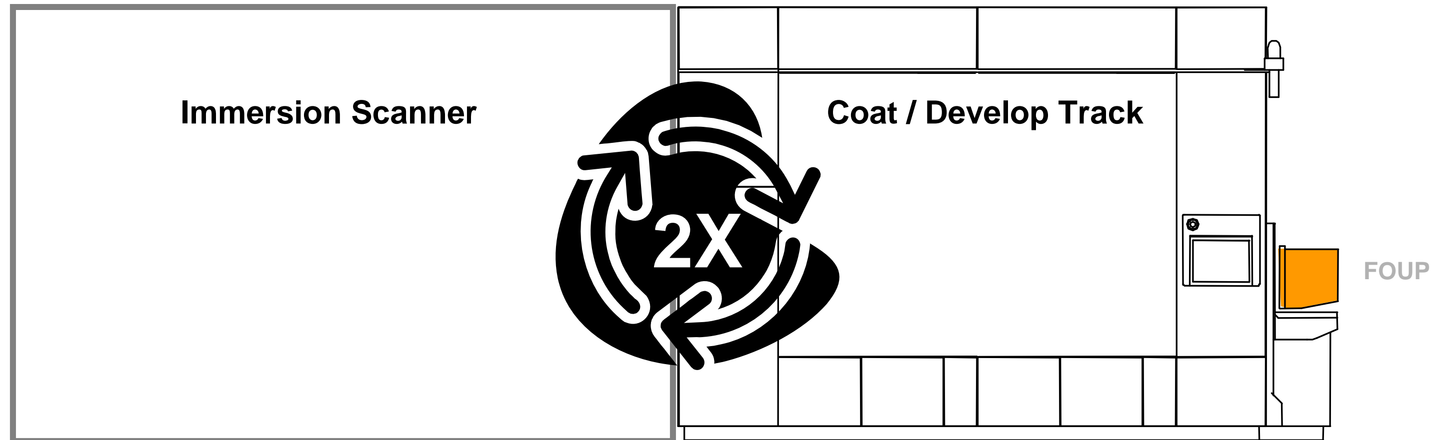
"Photo" Double Patterning = Two-Cycles Through Lithocell



- **Two-Cycle Wafer Flow Management Dilemma**
  - Semiconductor Fab Host reloads FOUP cassette for 2nd cycle or
  - Track internally manages auto-start of second cycle/pattern and communicated to scanner via linked-litho network

- **Solution: Clear protocol with fab host and track/scanner on second cycle DP wafer reloading**

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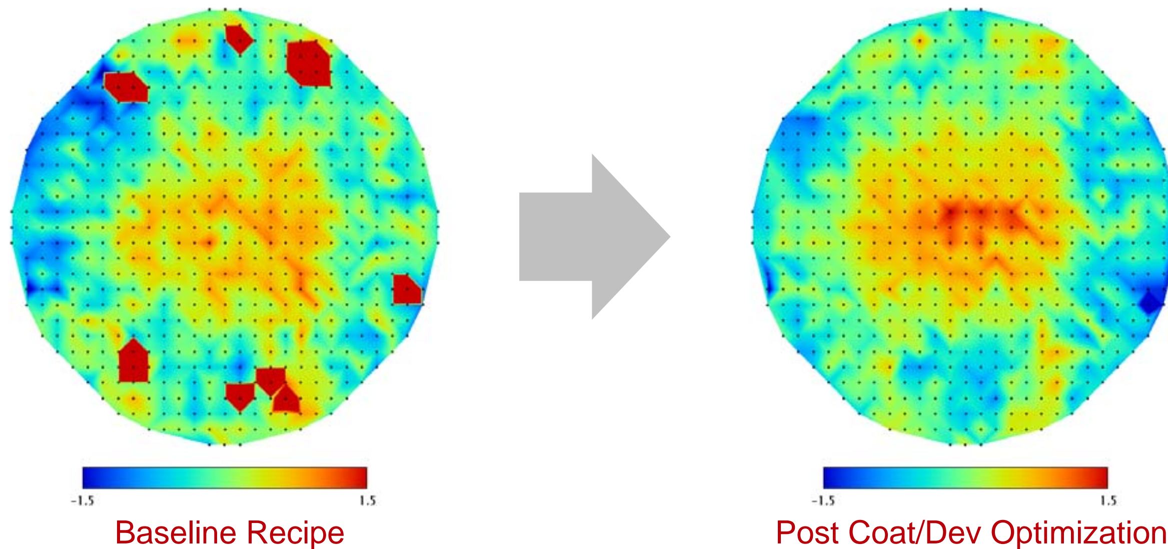
SOKUDO 22nm Double Patterning Process Development at IMEC

JSR Freeze Coat – Develop Process Optimization



Baseline Recipe

Post Coat/Dev Optimization

- **CDU & Defectivity was Unacceptable with Initial Baseline Process**
  - **Freeze Material was Not Properly Removed due to Poor Wetting**
- **Coat & Develop Optimization Complete: CDU ~1.5nm 3σ**
  - **Defects from Remaining Freeze Material Resolved**
- **Next… Evaluated cdTune™ at Freeze PAB to Optimize CDU**
  - **Model Predicts ~1nm 3σ**

All Results Single Pattern Only

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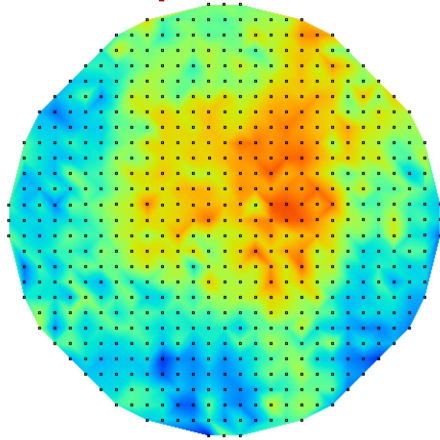
Resist #1 CDU Tuning

Post-FZX CDU Tuning

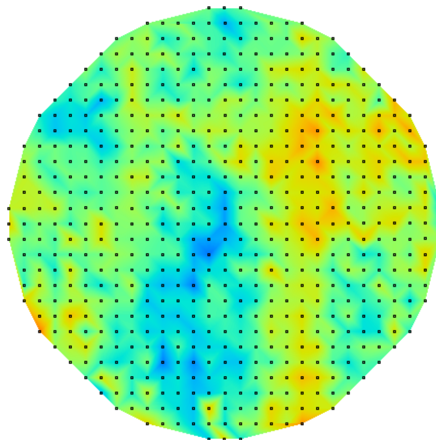
POR Wafers
Temp. Unif. PEB



-1.2 1.2

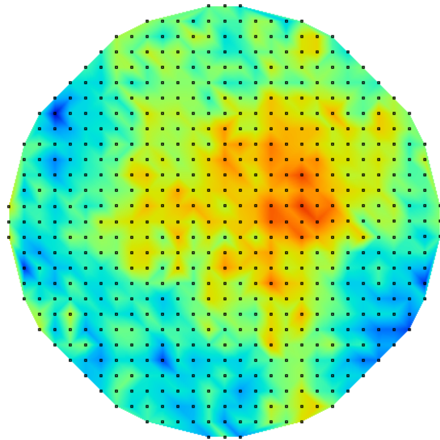
3σ=1.15nm

BHP
cdTune



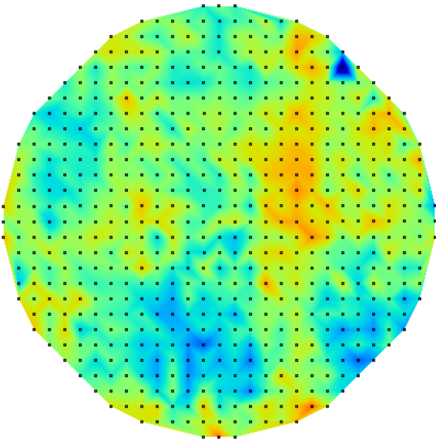
-1.2 1.2

3σ=0.93nm



-1.2 1.2

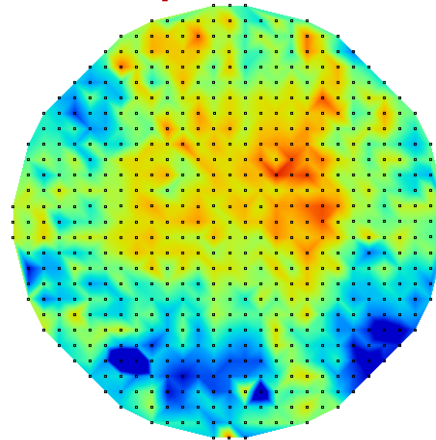
3σ=1.29nm



-1.2 1.2

3σ=0.86nm

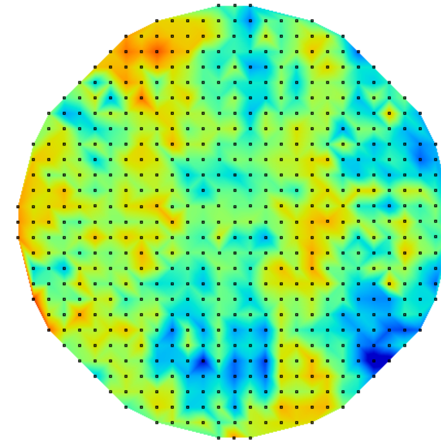
POR Wafers
Temp. Unif. PAB



-1.2 1.2

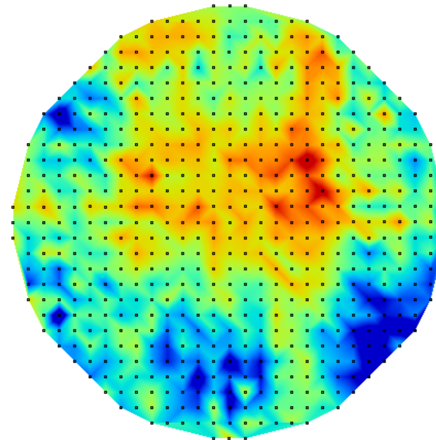
3σ=1.38nm

BHP
cdTune



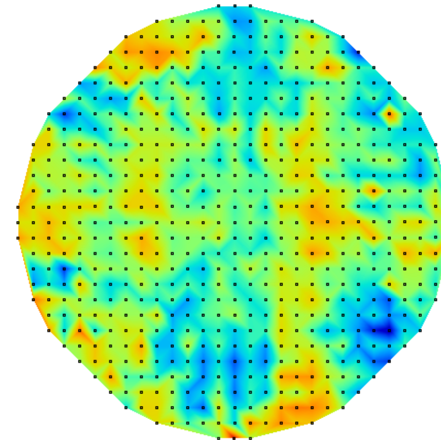
-1.2 1.2

3σ=1.10nm



-1.2 1.2

3σ=1.56nm

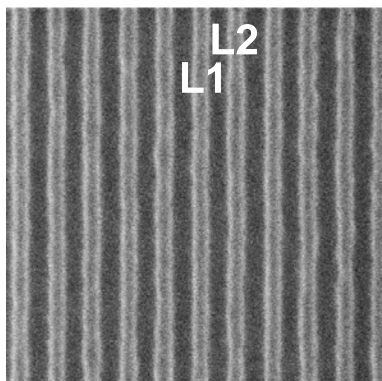


-1.2 1.2

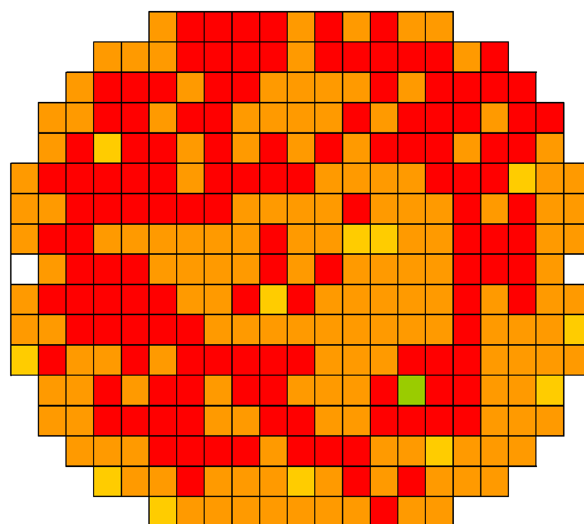
3σ=1.14nm

TOK "Freeze Free" DP, 32nm HP CDU Results

Data courtesy of IMEC & TOK

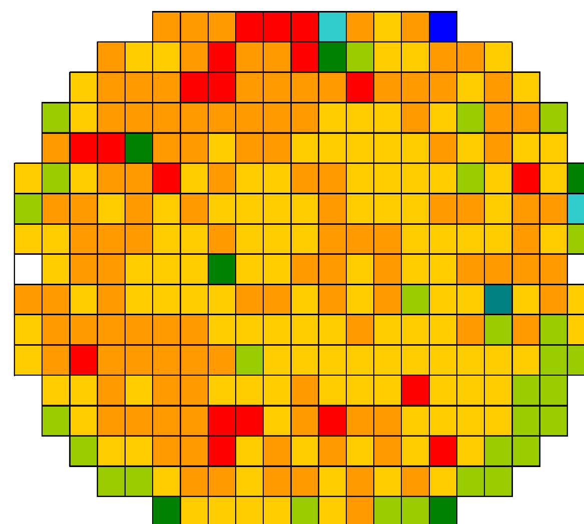


L1 CDU

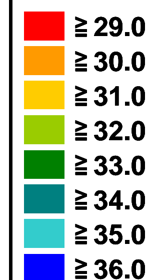


Ave. CD	30.1nm
3σ	1.45nm
Ave. LWR	3.76nm

L2 CDU



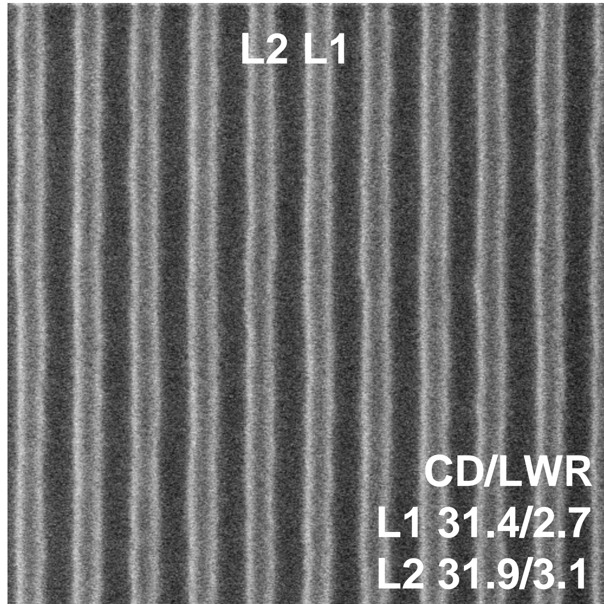
Ave. CD	31.2nm
3σ	2.74nm
Ave. LWR	4.54nm



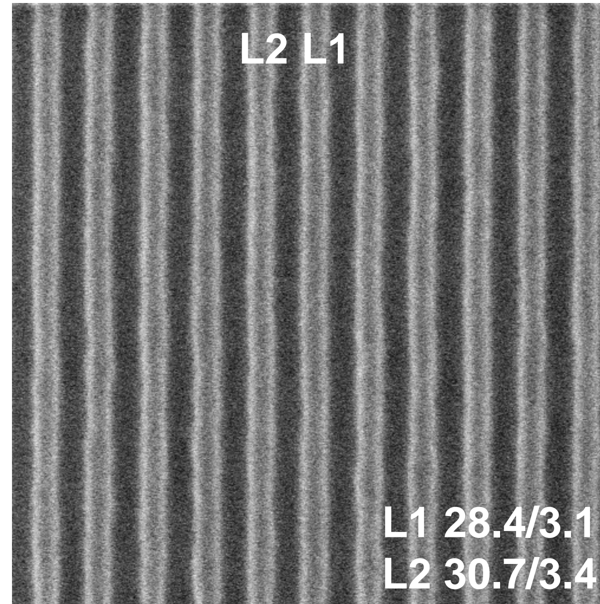
- Target: 32nm DHP
- Film thickness was optimized to prevent pattern collapsing
- CDU indicated applicable value to further investigations

TOK "Freeze Free" DP @ NA 1.0 dipole

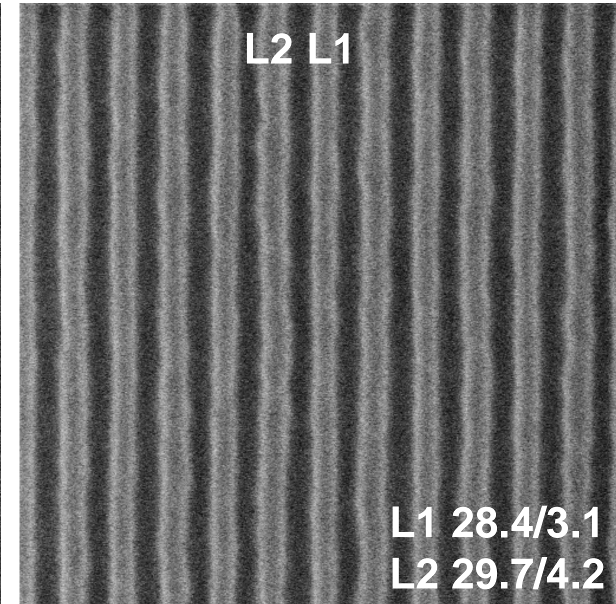
32nm DHP



30nm DHP



28nm DHP



- **Target: 32nm DHP**
- **Film thickness was optimized to prevent pattern collapsing.**
  → Thinner setting both 1st level resist and 2nd level resist.
- **30 & 28nm HP patterns were obtained utilizing dipole illumination.**

Data courtesy of IMEC & TOK

Key Message: SOKUDO DUO for Double Patterning

- **SOKUDO DUO Immersion Track Qualifying @ 250wph**
- **SOKUDO DUO flexible to meet >200wph requirement for multiple Double Patterning Alternatives**
- **SOKUDO on the leading-edge of Double Patterning process know-how in collaboration with IMEC**

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