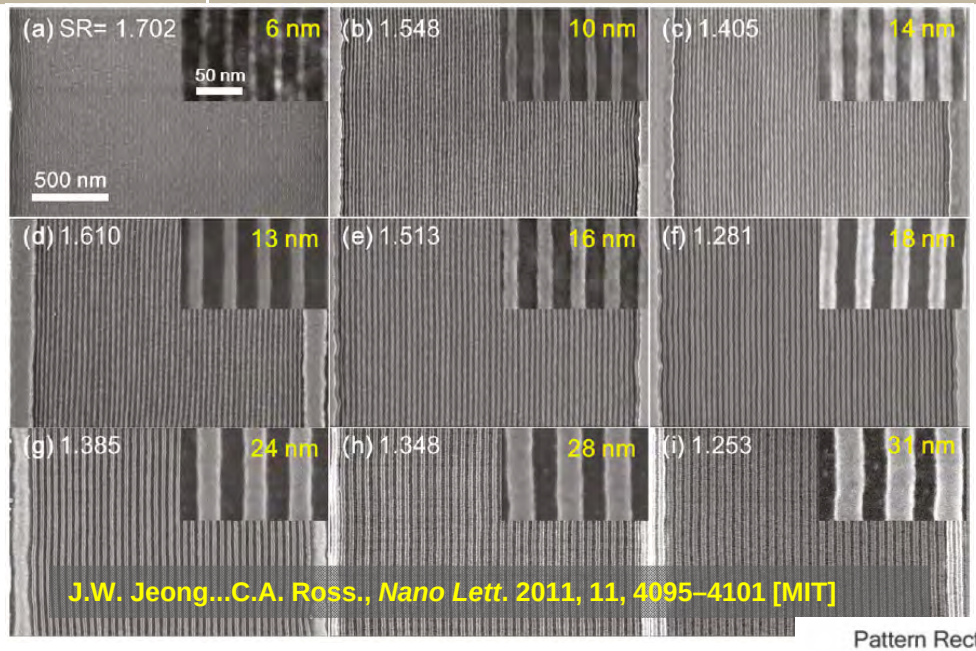
Stanford University

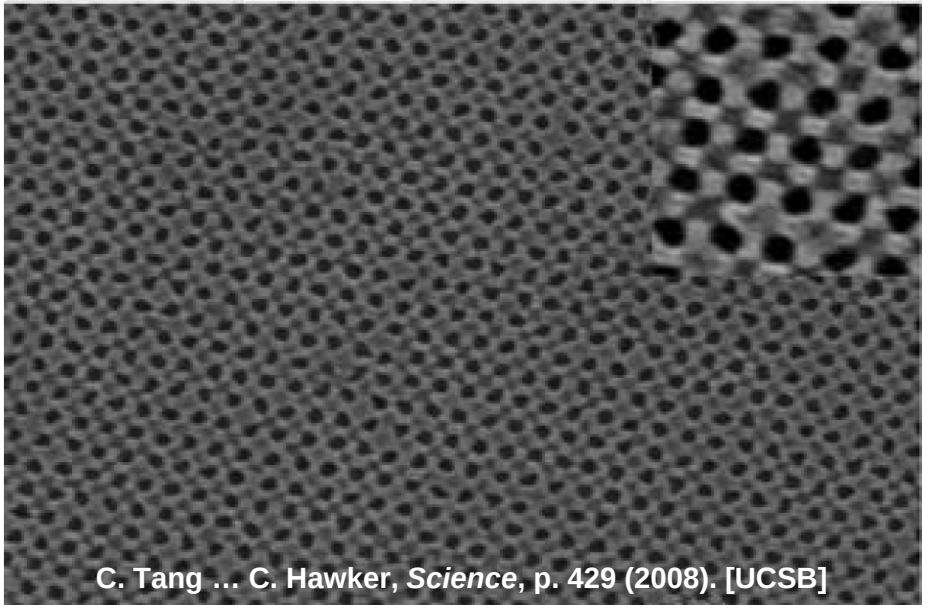
Directed Self-Assembly for the Semiconductor Industry

H.-S. Philip Wong, Chris Bencher[#]
Linda He Yi, Xin-Yu Bao, Li-Wen Chang

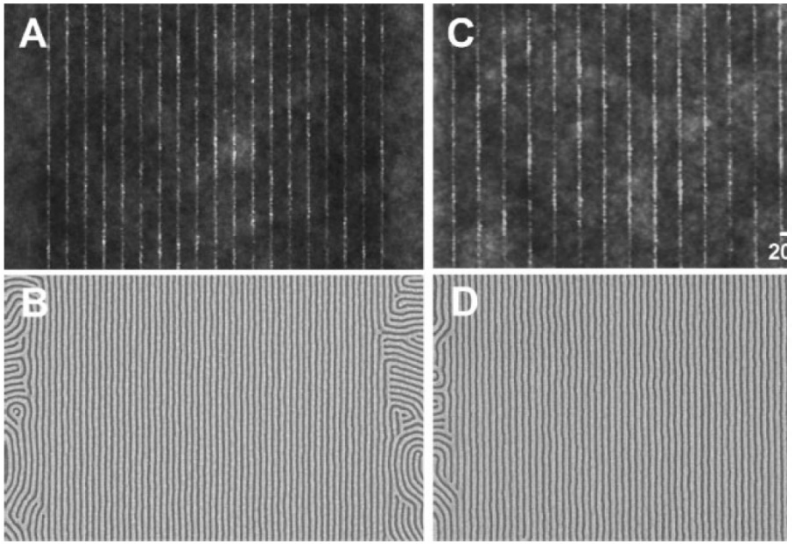
Stanford University, [#]Applied Materials



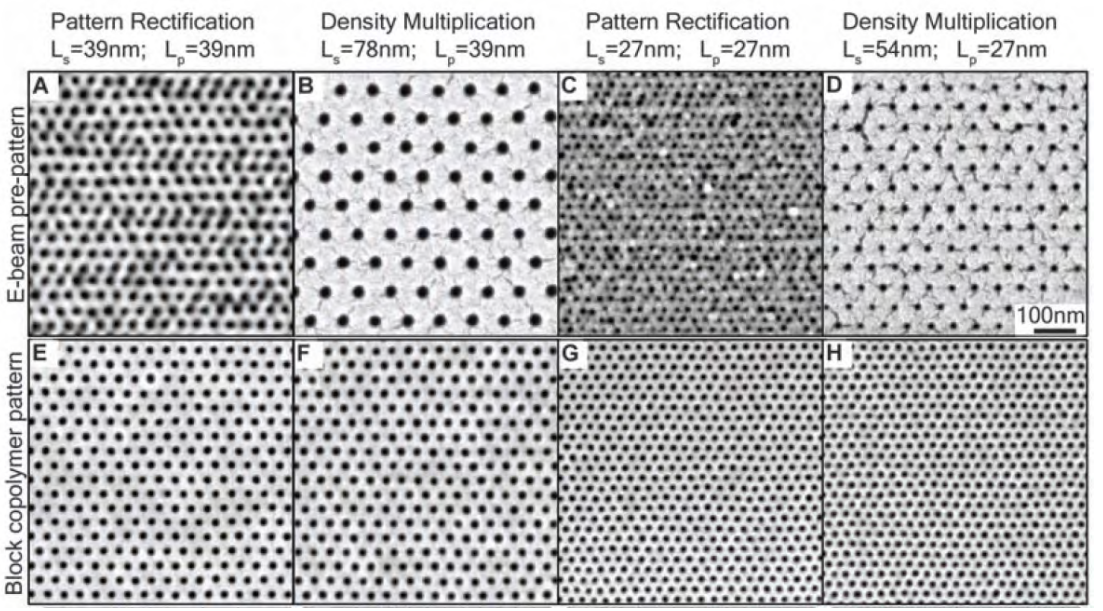
J.W. Jeong...C.A. Ross., *Nano Lett*. 2011, 11, 4095–4101 [MIT]



C. Tang … C. Hawker, *Science*, p. 429 (2008). [UCSB]



J. Y. Cheng et al., *Adv. Mater*. 2008, 20, 3155–3158 [IBM]



R. Ruiz…P. Nealey, *Science* ***321****, 936 (2008)* [Hitachi, Wisconsin]

Device Fabrication

Does not require long range order

J. Stork, TI (2007), Stanford seminar

Device Fabrication Requires

- Multiple-pitch
- Multiple-ordering
- Multiple-size
- One layer process
- Single material system
- Industrial compatible process
- Transparent to circuit designers

Technical requirement

Practicality (i.e. cost)

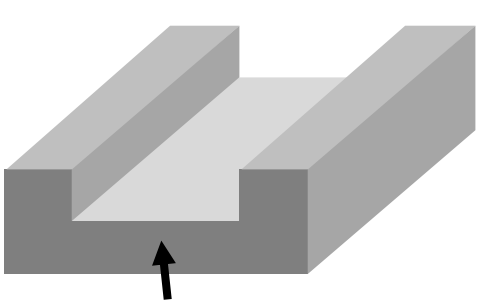
Nangate cell library, http://www.nangate.com

J. Stork, TI (2007)

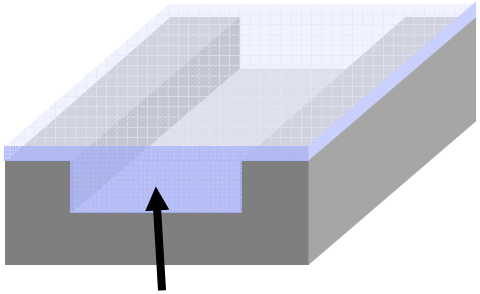
Why don’t we place the shapes where we want them to be?

Adapted from: ucsusa.org

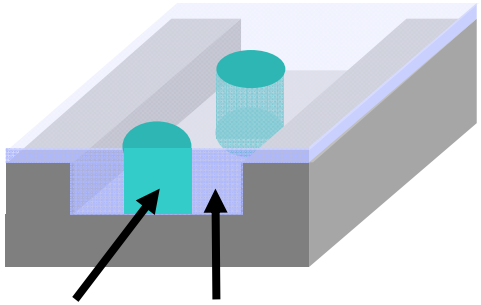
Directed Self-Assembly by Physical Confinement



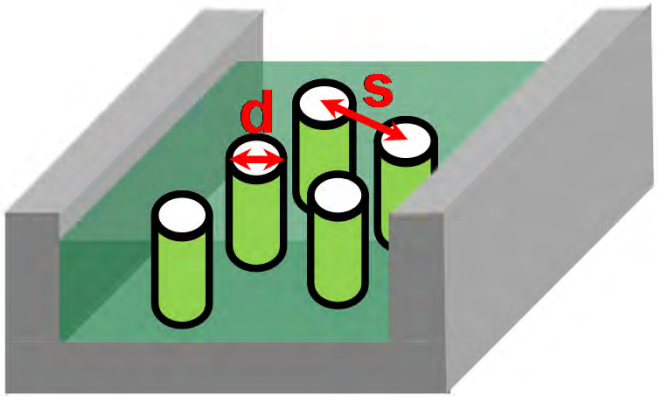
Guiding Template: Physical Confinement

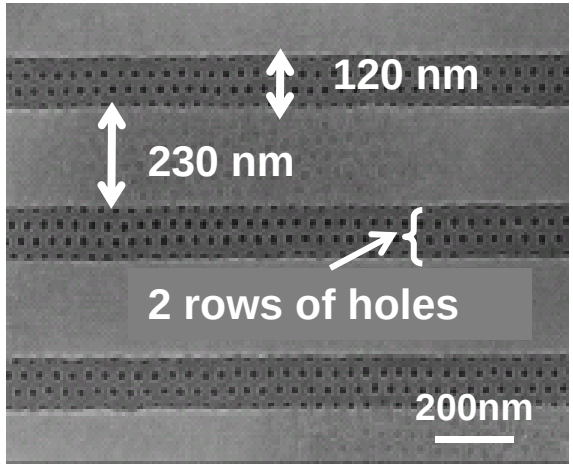


PS-*b*-PMMA



PMMA **PS**

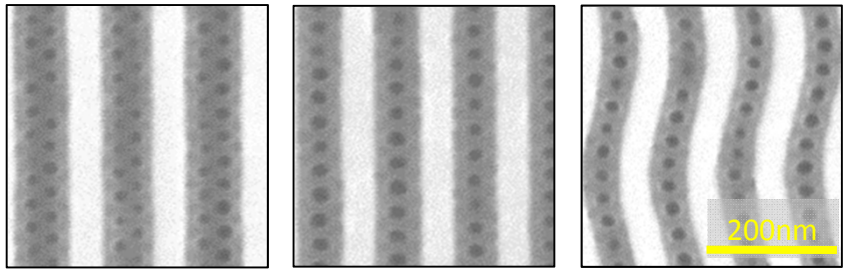




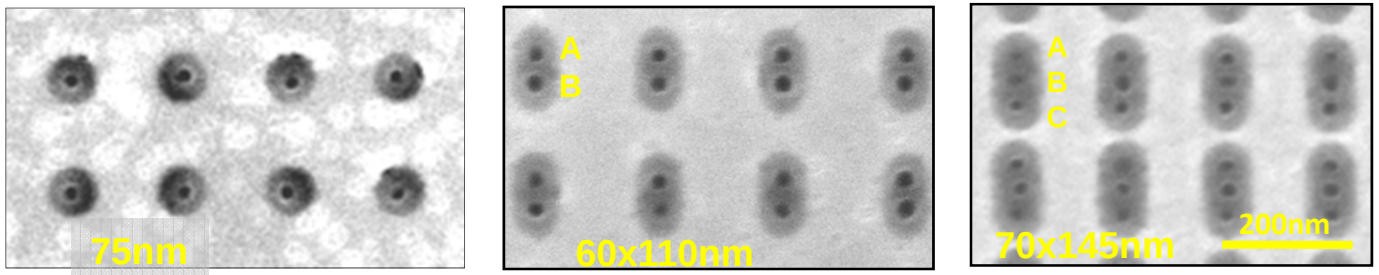
L.-W. Chang…H.-S. P. Wong, *IEDM* , p. 879, 2009

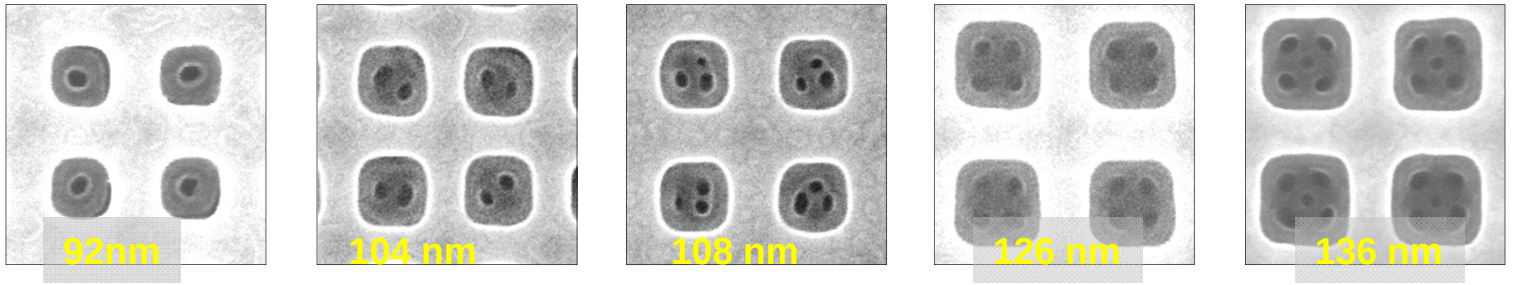
Control of DSA with Small Guiding Templates

- **Size Comparable to self-assembly dimensions**

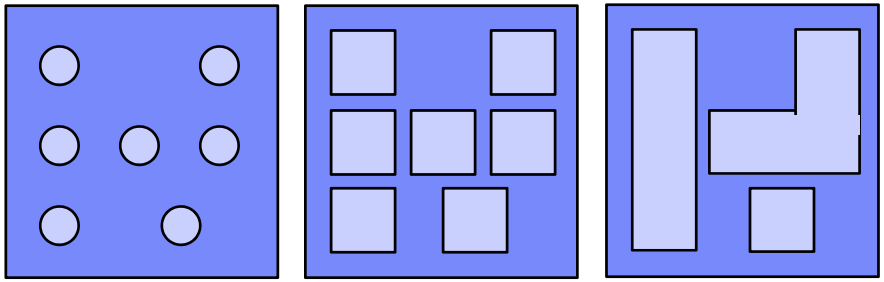


Flexible and precise control knobs: Thickness, size, density





Small Templates

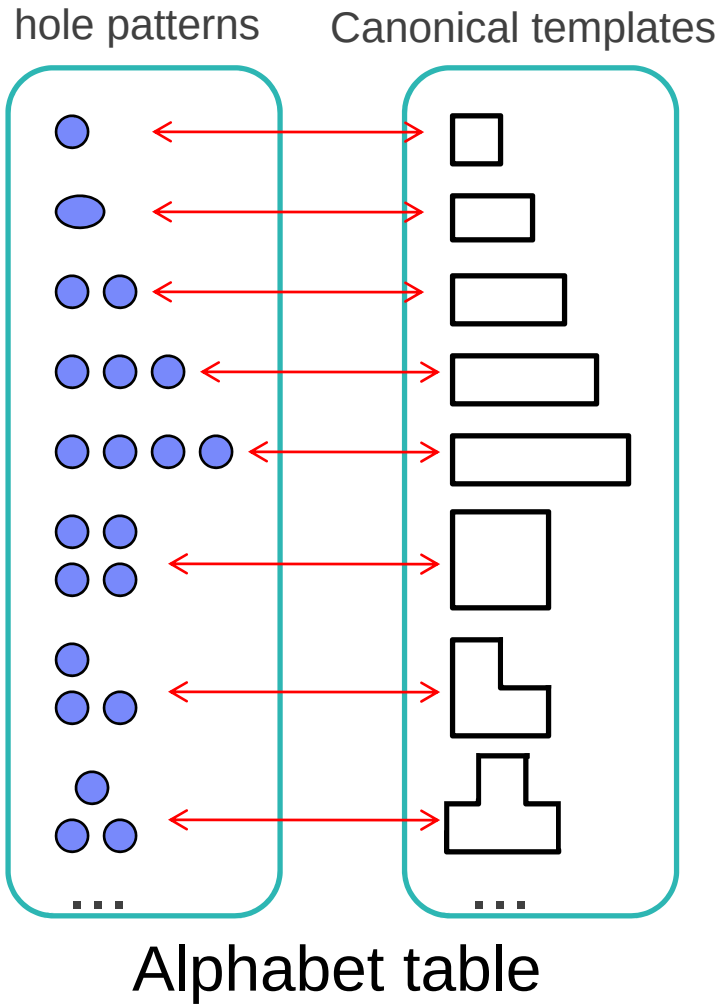


Canonical templates:

- Simplest template set to form desired patterns
- Manufacturable with current litho tech.

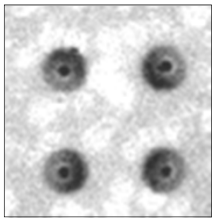
Design Rules:

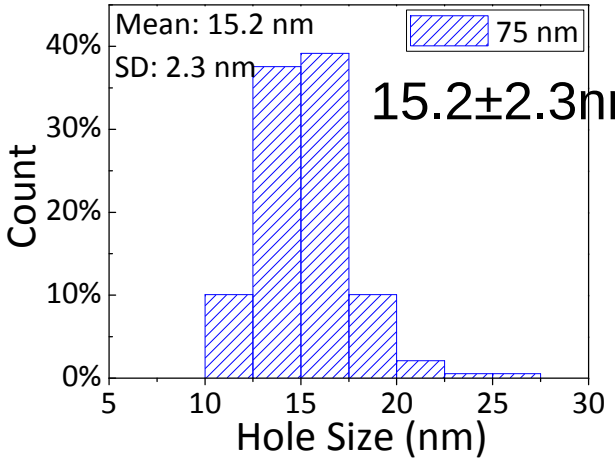
- The standards to disassemble a layout to canonical templates and reassemble canonical templates to pattern devices

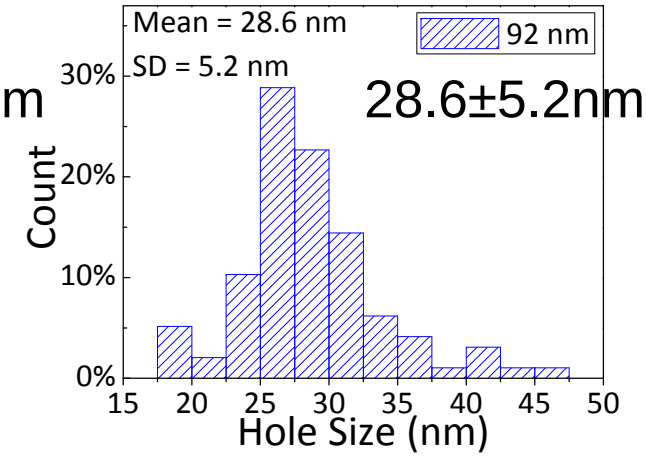


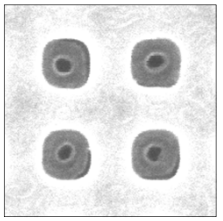
Alphabet table

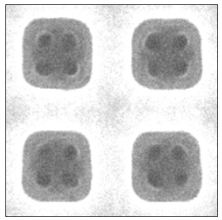
Square Template DSA Pattern Size Analysis

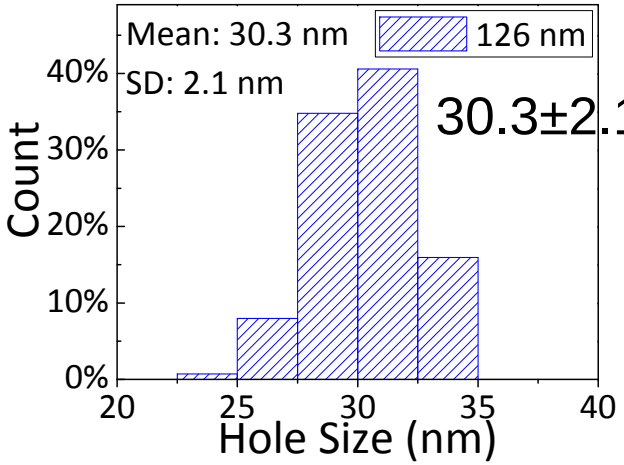


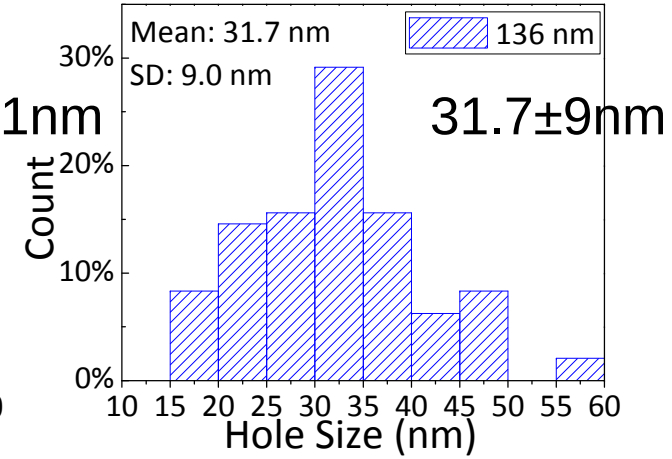


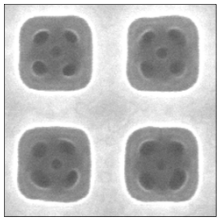






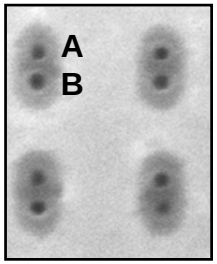


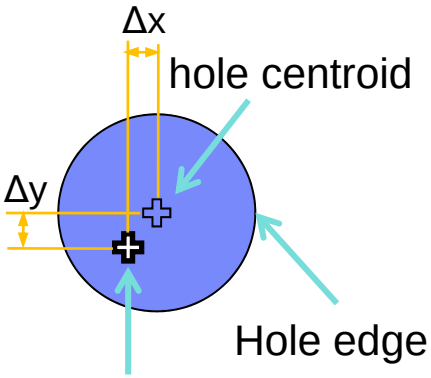




H. Yi … H.-S. P. Wong, *Adv. Mater.* , 2012

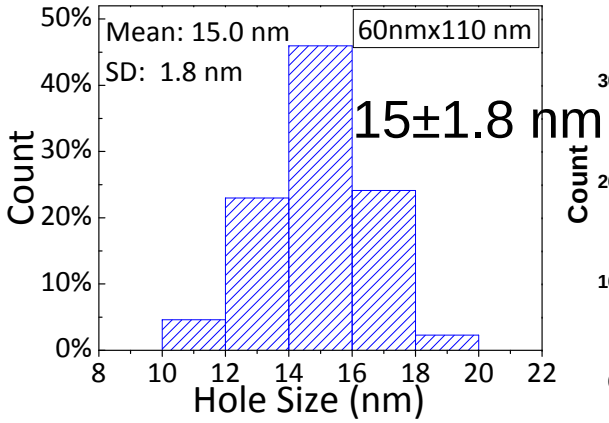
2-Hole Pattern Analysis

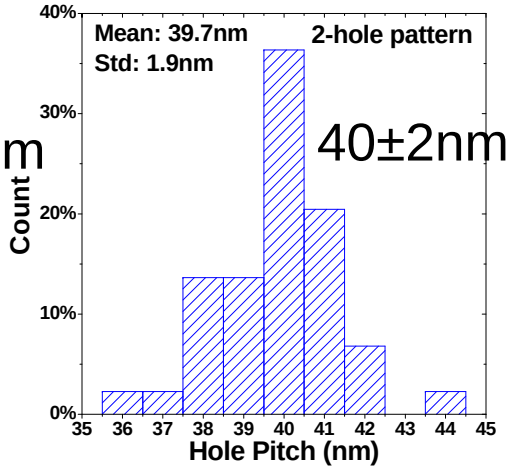


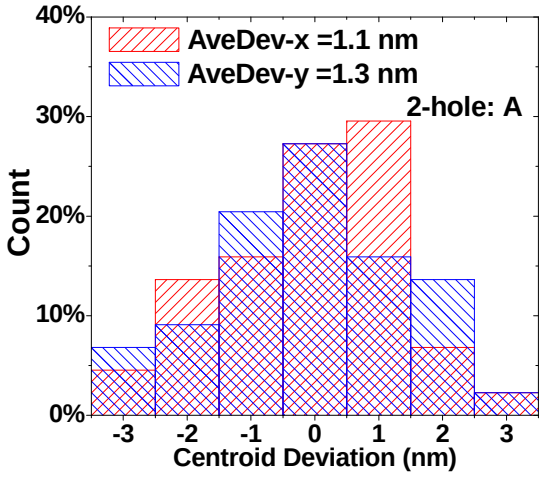


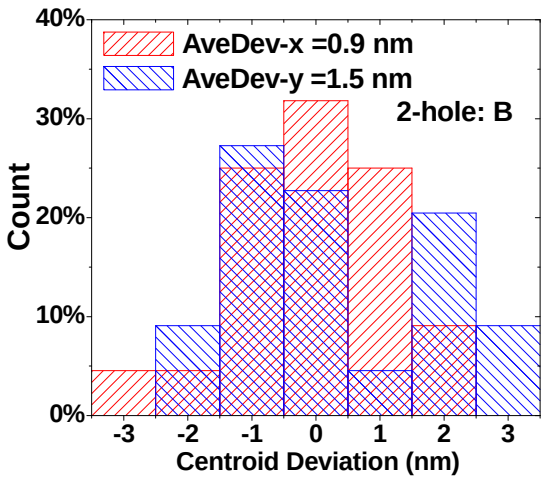
Average centroid

Overlay accuracy: Average absolute deviation





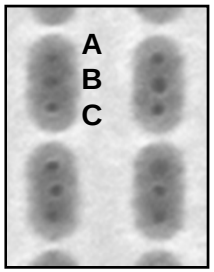


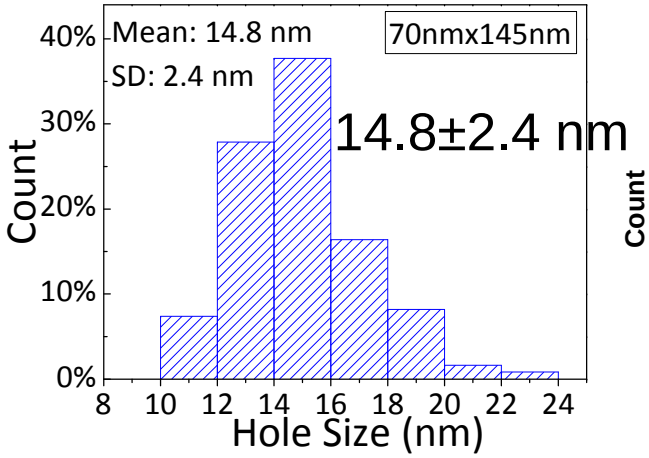


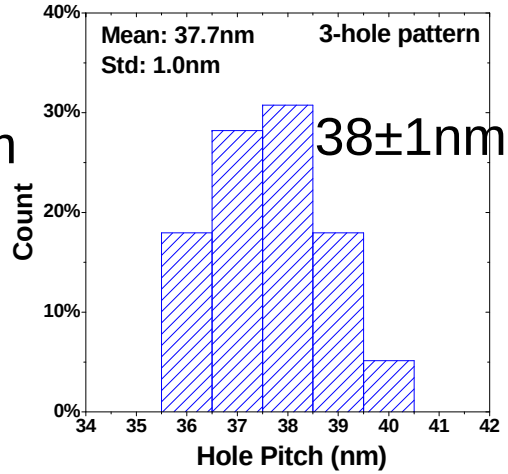
Δx ~1nm
Δy ~1.5 nm

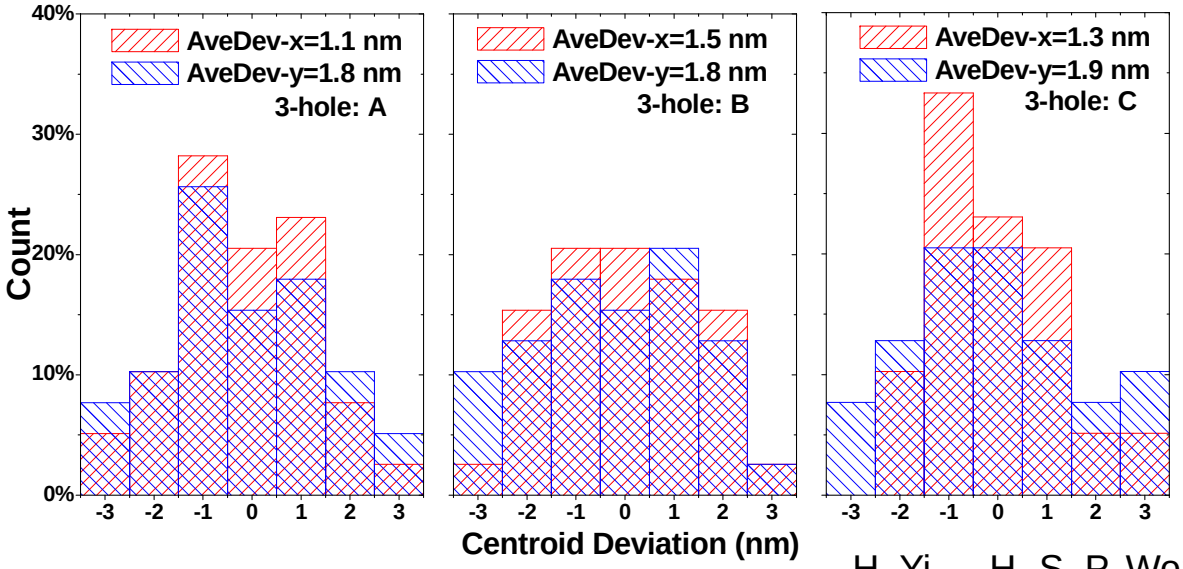
H. Yi … H.-S. P. Wong, *Adv. Mater.* , 2012

3-Hole Pattern Analysis





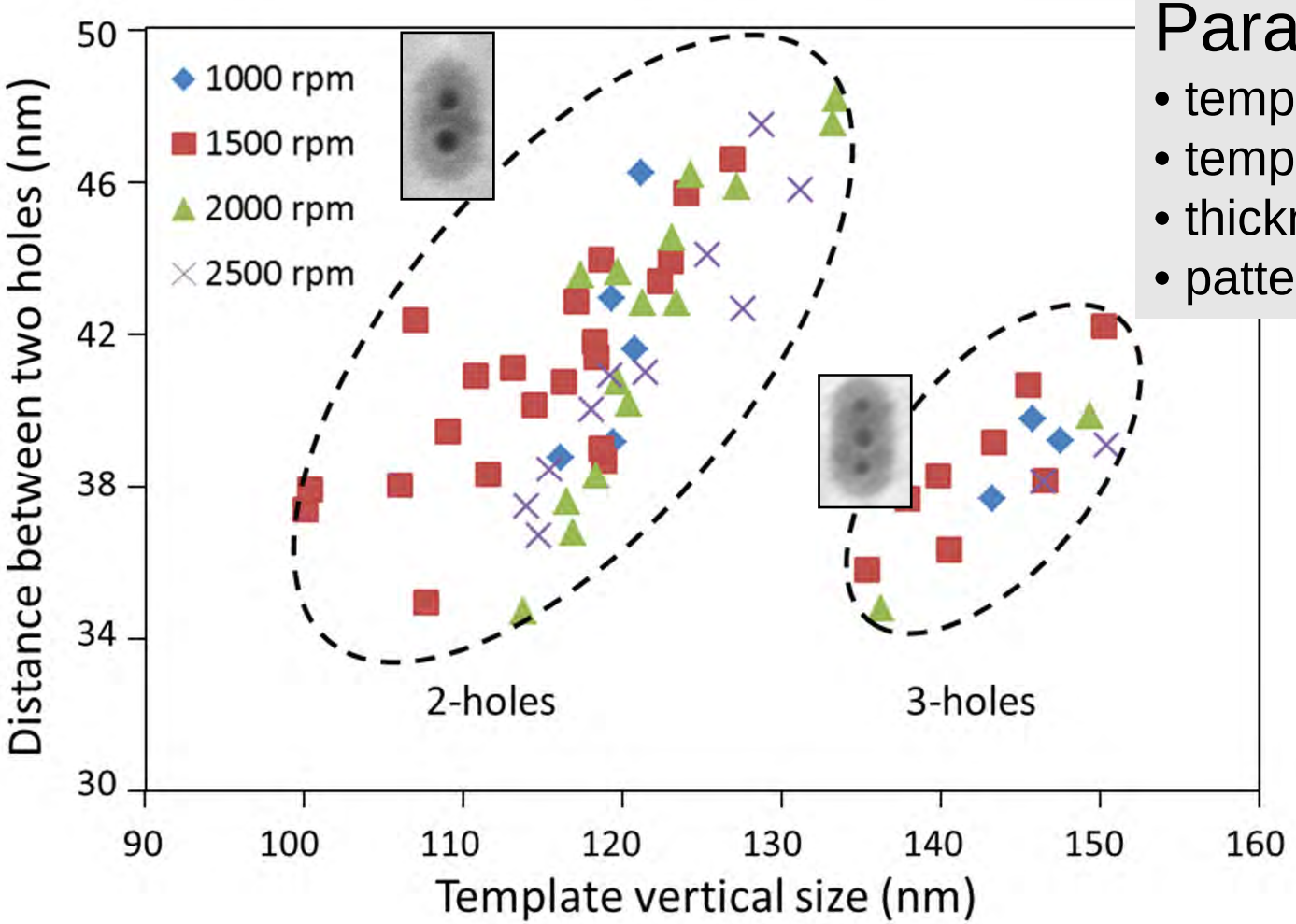




Δx ~1.5 nm
Δy ~1.9 nm

H. Yi … H.-S. P. Wong, *Adv. Mater.* , 2012

Design Space for 2-3 Hole Guiding Templates

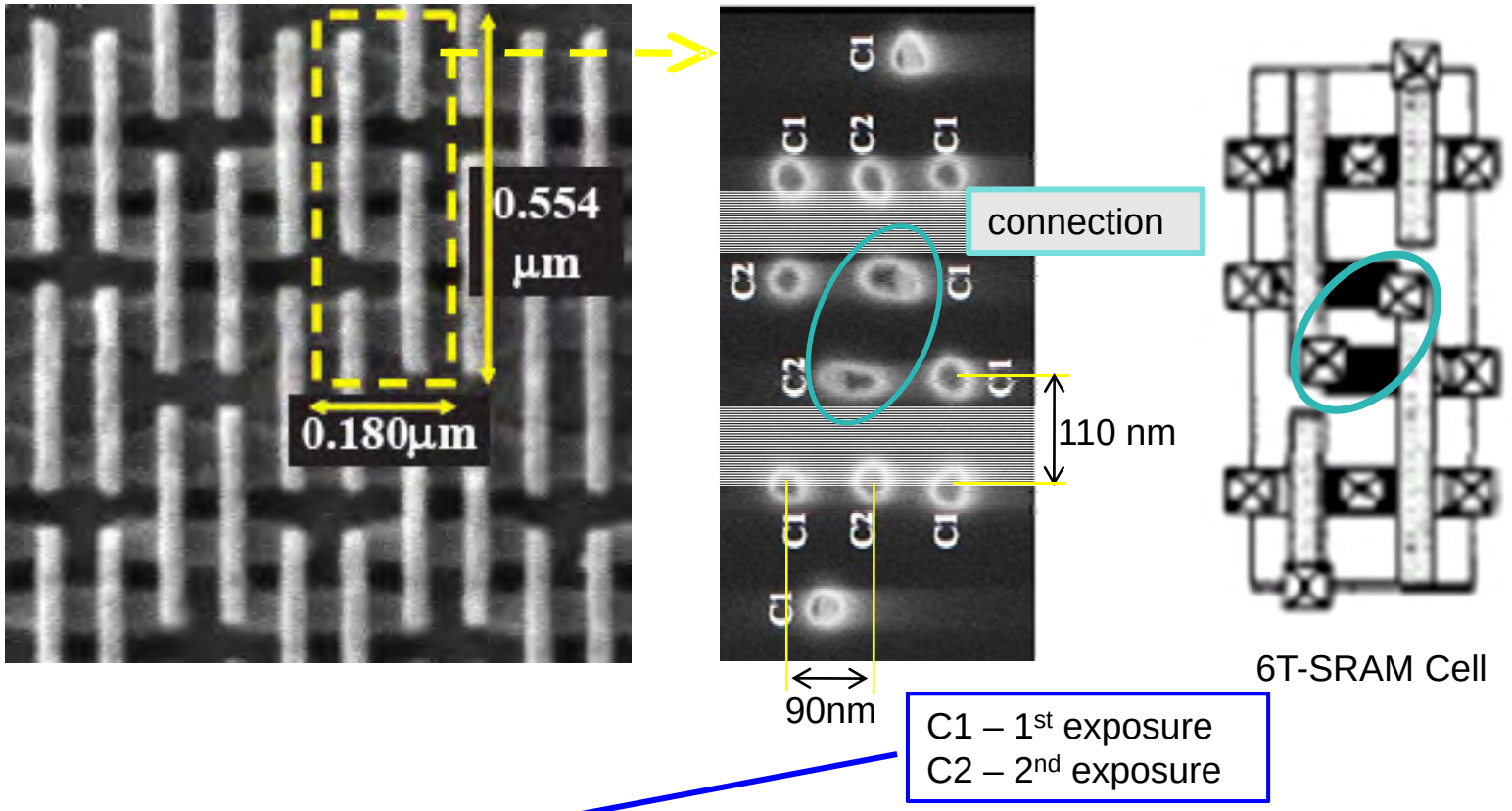


Parameters:

- template size
- template shape
- thickness
- pattern density

H. Yi … H.-S. P. Wong, *Adv. Mater.* , 2012

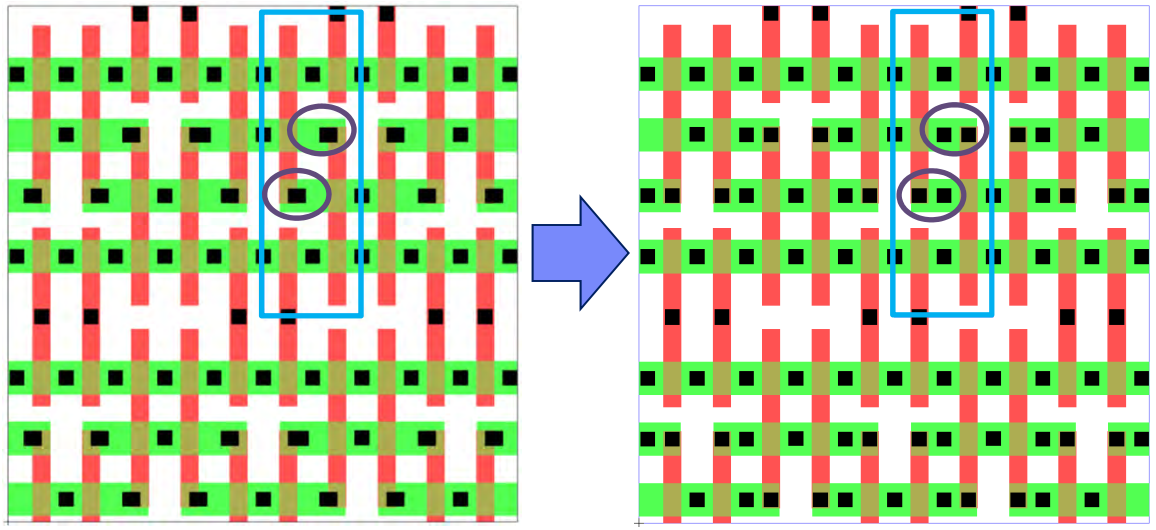
IBM 22-nm SRAM Contact Holes Layout



*Double pattern and double etch process were used to achieve these 26 nm size contact holes.

Haran, B. S. Proc. IEDM (2008).

DSA-Aware Contact Holes for SRAM

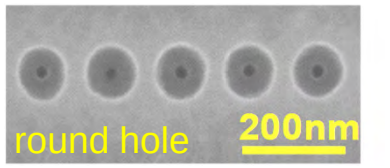


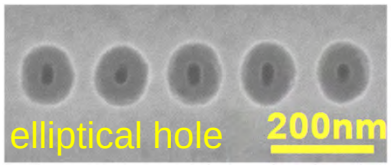
Active region

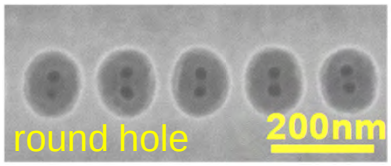
Polysilicon gate

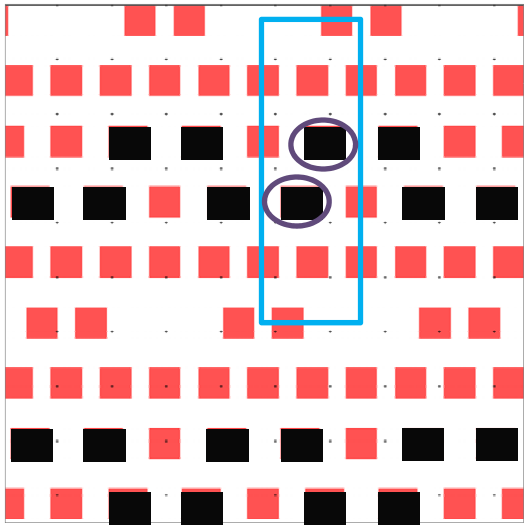
Contact hole

Connection







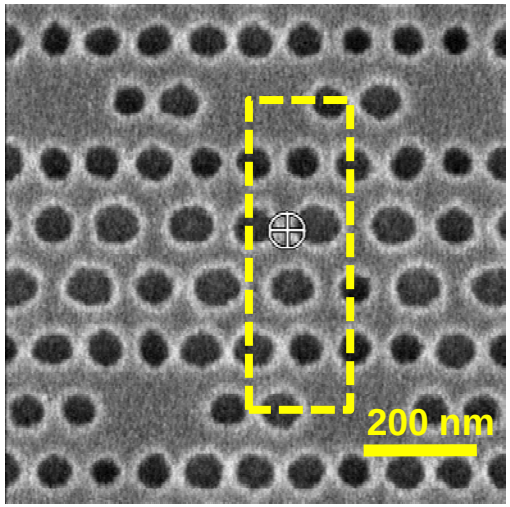


Template mask layout

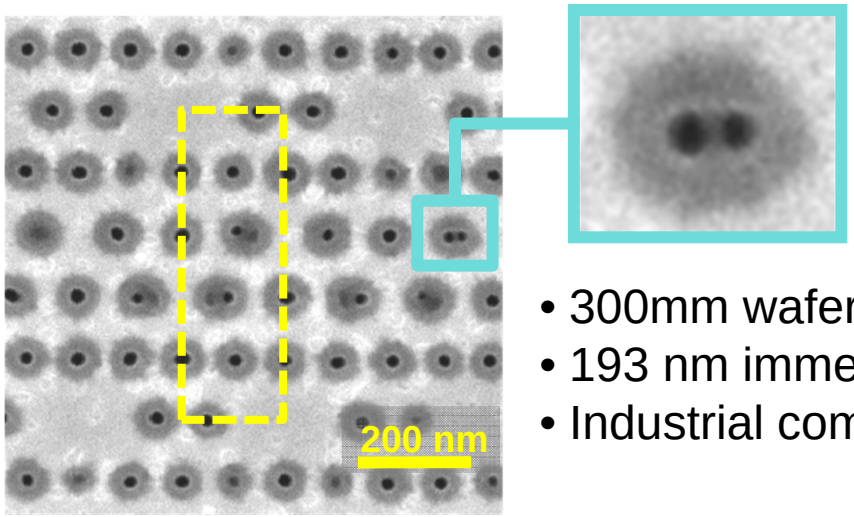
Size: 56nm (contacts)
56 x 70 nm (connection)
Pitch: x-axis=90nm
y-axis=110nm

DSA Patterned Contact Holes for SRAM

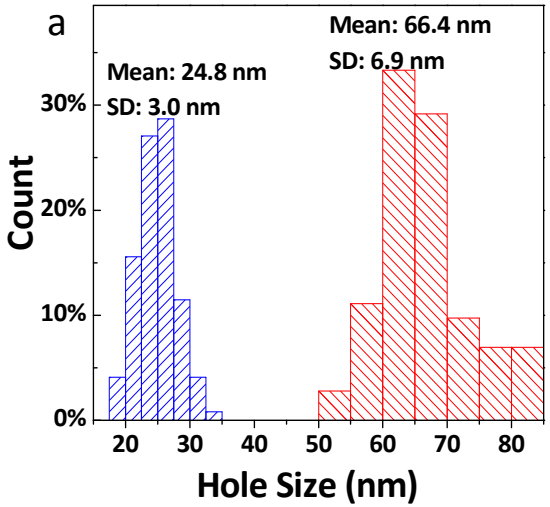
Template SEM

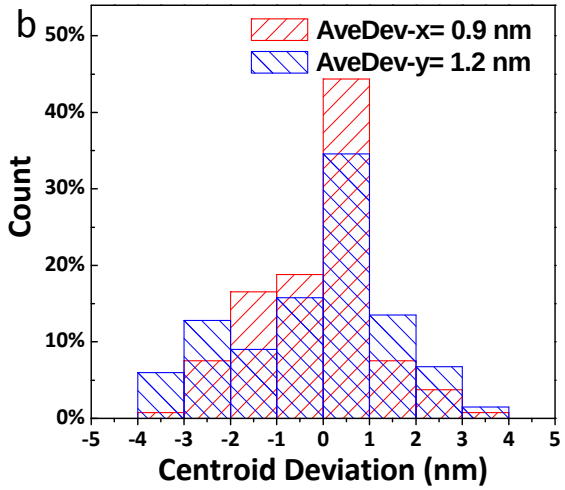


DSA SEM



- 300mm wafer
- 193 nm immersion Litho
- Industrial compatible sol.





Template ~ 66.4±7nm

Contact hole ~ 25±3nm

Centroid Δx ~0.9 nm

Centroid Δy ~1.2 nm

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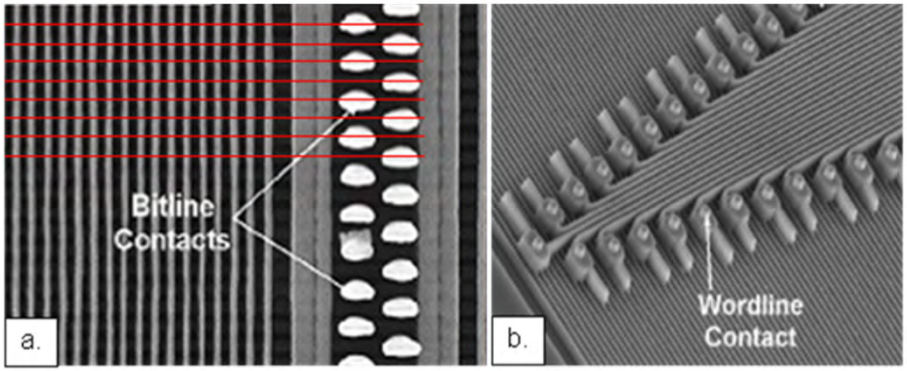
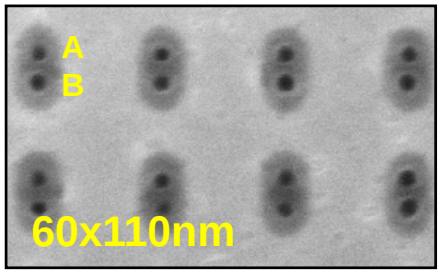
Contact Holes for NAND (strategy)

2-hole templates for NAND

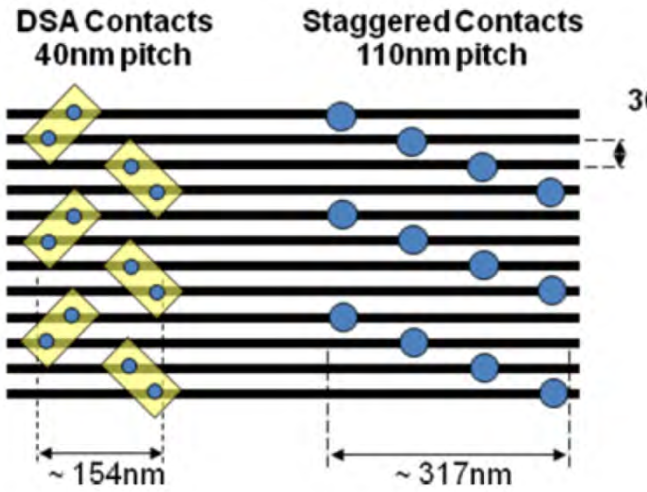


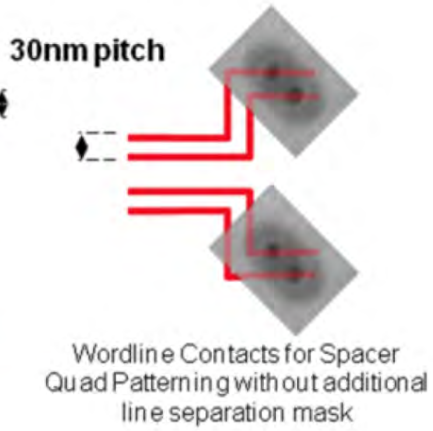


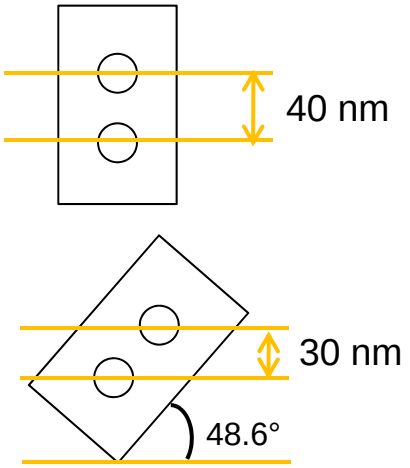
15 nm hole size
40 nm pitch

(*source: UBM Techinsights*)

Rotate to fit 30nm pitch







Extend to 15-nm NAND

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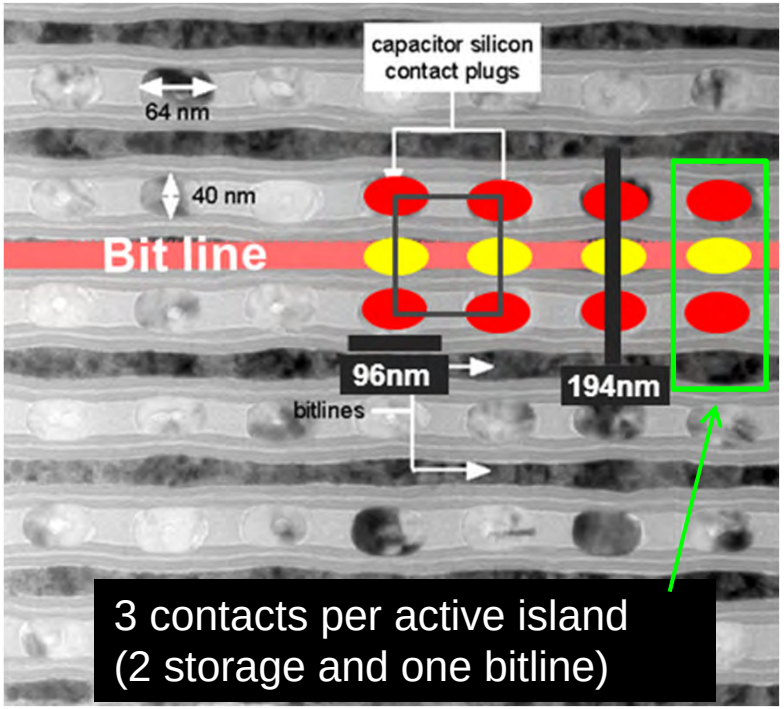
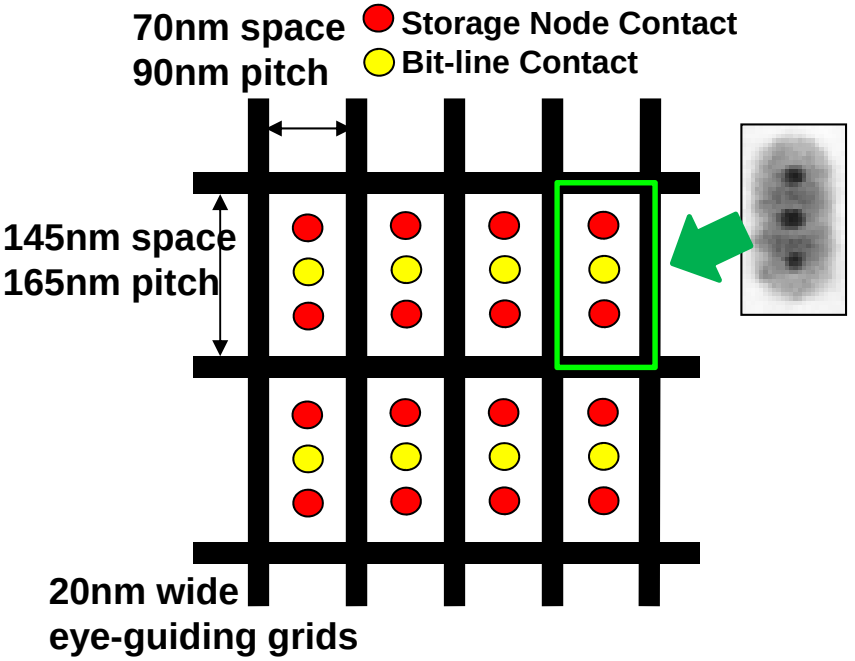
Contact holes for DRAM (strategy)

3-hole templates for DRAM



Example of 3x-nm DRAM
(*Source: Chipworks*)



Shrink to 2x-nm DRAM
3-hole templates (70x145nm)

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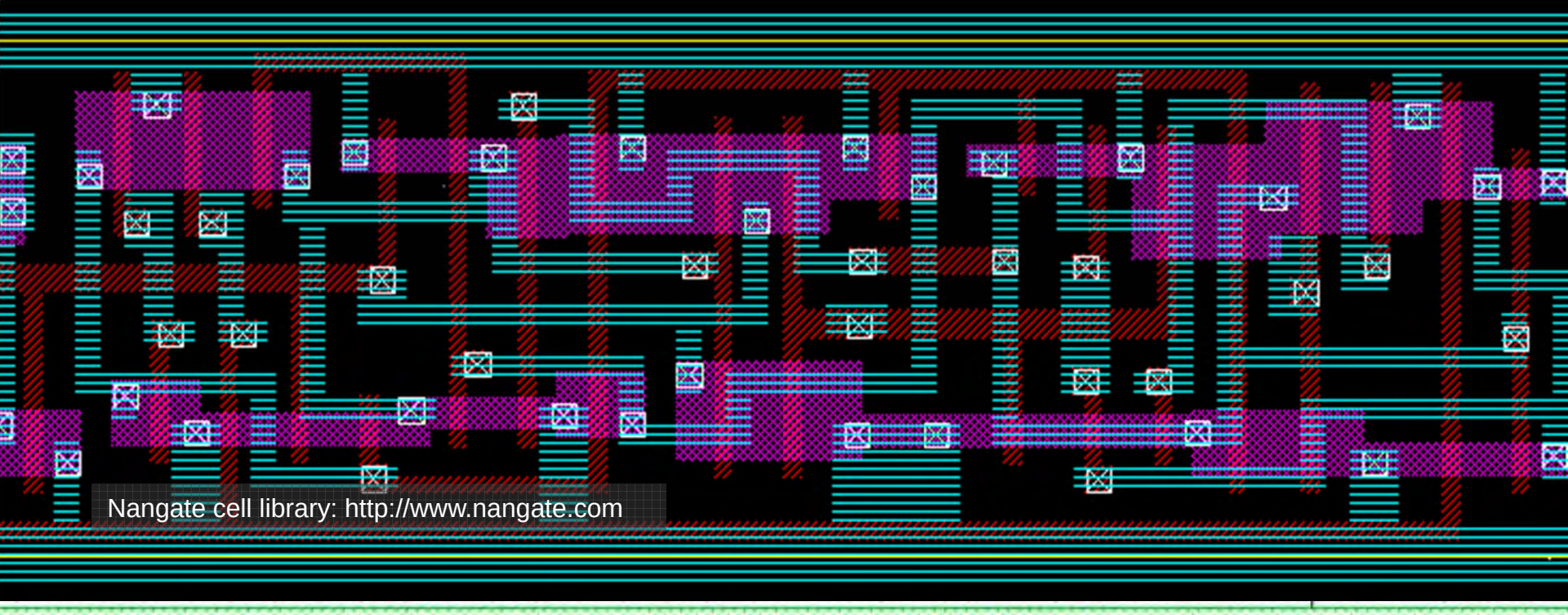
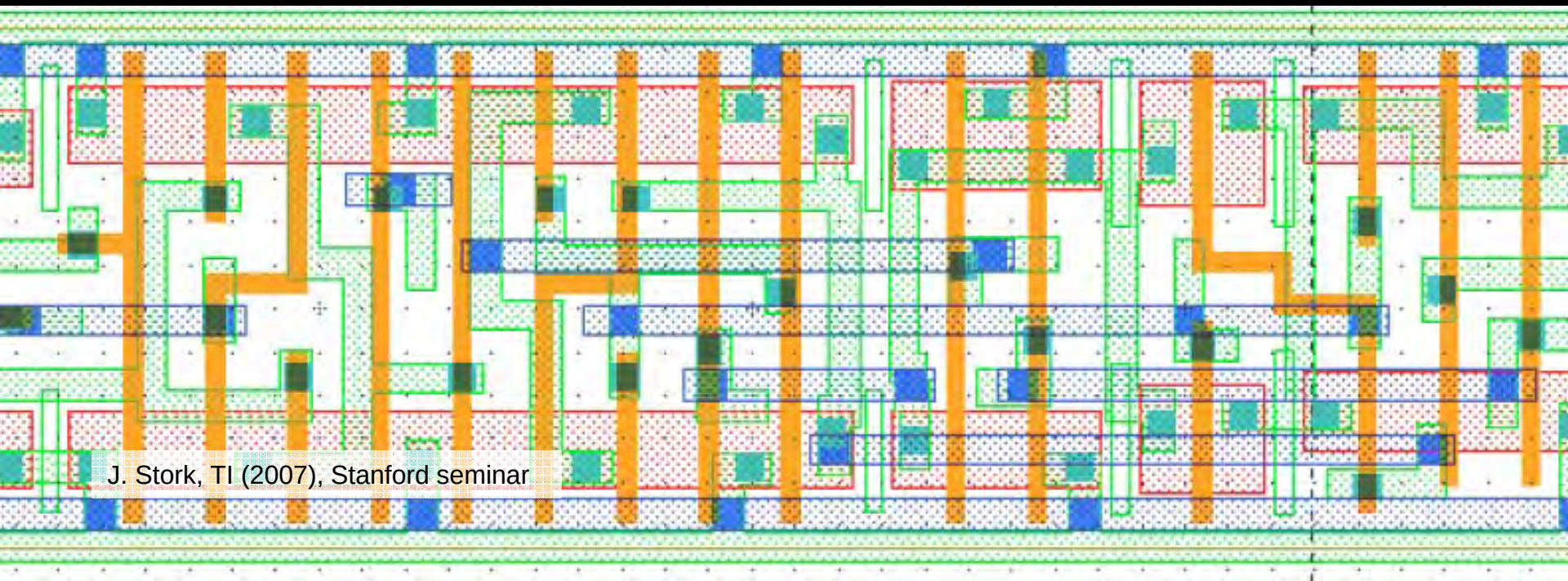
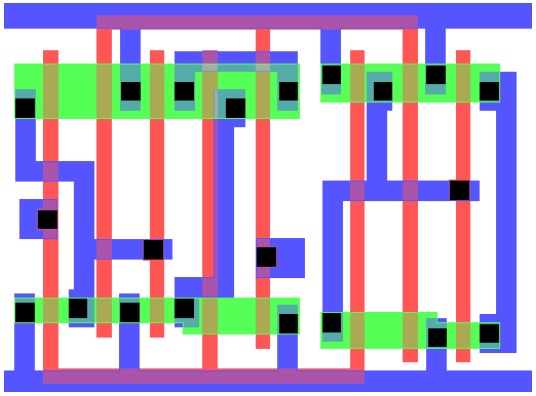

Nangate cell library: http://www.nangate.com


J. Stork, TI (2007), Stanford seminar

Contacts for Random Logic Circuit

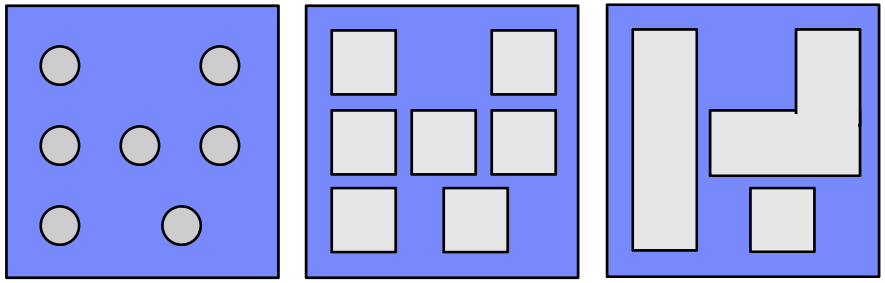
Example: Conventional 45nm HA-X1 Layout



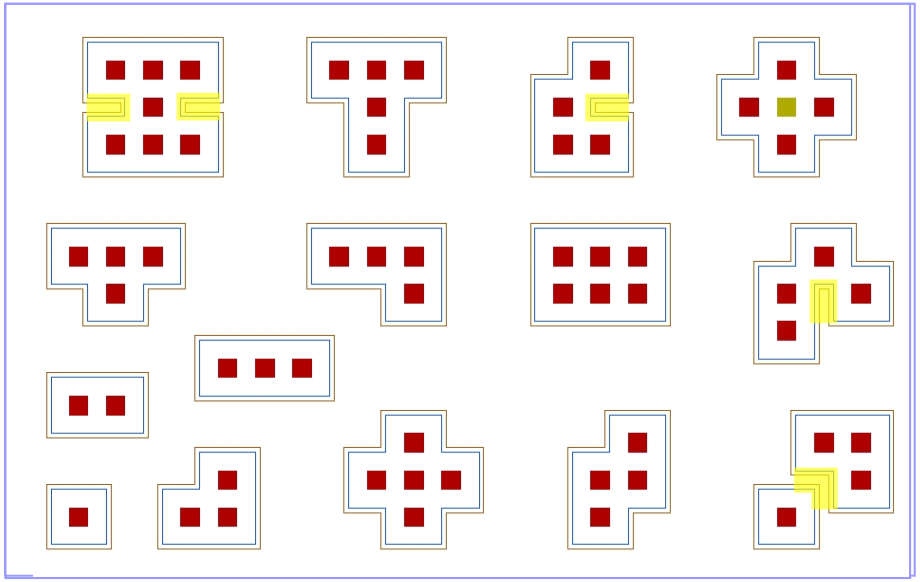
Source: Nangate 45nm Open Cell Library

Challenges for DSA patterning

- Overcome resolution limits
- Irregular contact distribution
- Guiding template design
- Optimal template size and shape



Contact hole layout **Design 1** **Design 2**



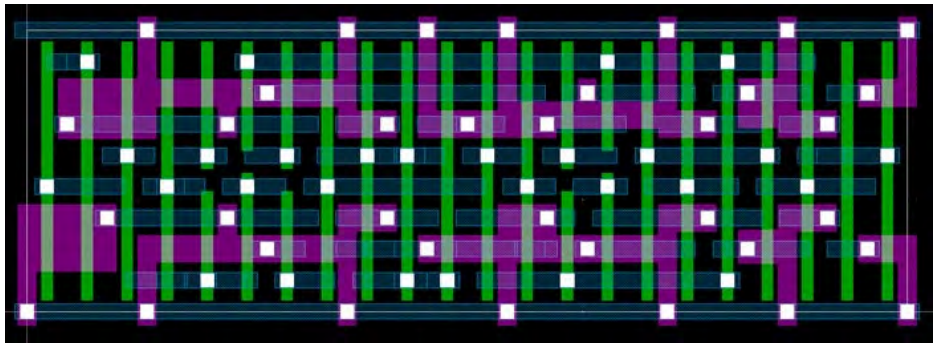
Courtesy of Jason Sweis, Cadence Design Systems

DSA-Aware Layout: Simplifying Template Design

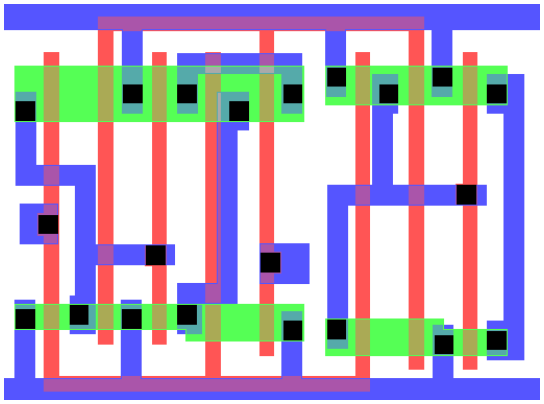
Starting Point:
Gridded **D**esign **R**ule (GDR)

- Lines: parallel, single width & pitch
- Contacts: positioned only at pre-determined grid points

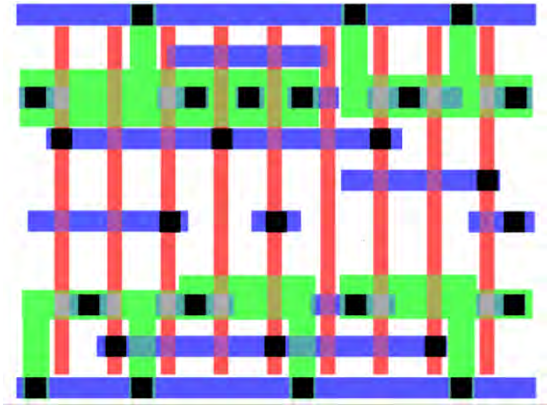
Scan-D Flip Flop designed with Gridded Design Rules



Source: http://www.tela-inc.com



Conventional HA-X1 Layout



DSA-Aware HA-X1 Layout

- Transistor sizes and connections (pin-out) unchanged
- No area penalty

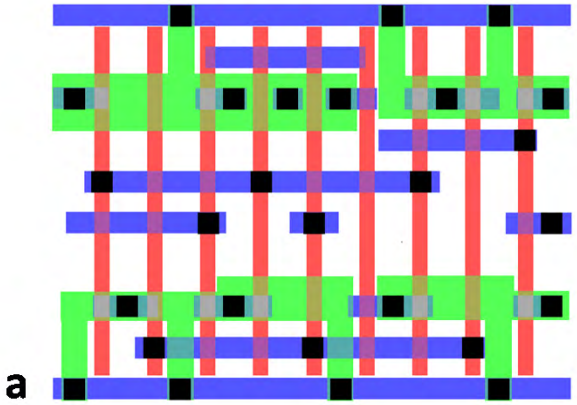
Metal 1 Poly Active Region Contact

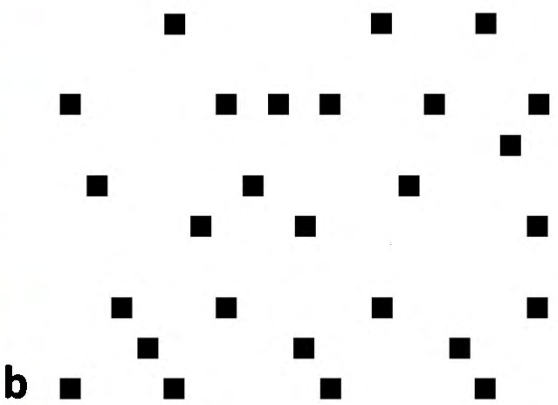
M2 vertical direction routing not shown for the sake of clarity

Random Logic Circuit Patterning: 1-bit Half Adder

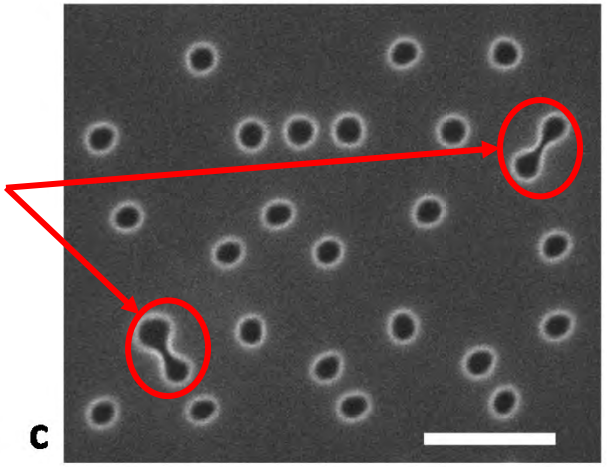
DSA-aware HA-X1

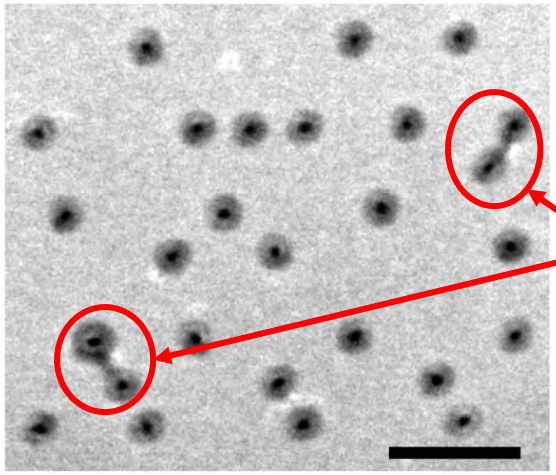
Contact Hole Layout





Template defects





DSA heal defects

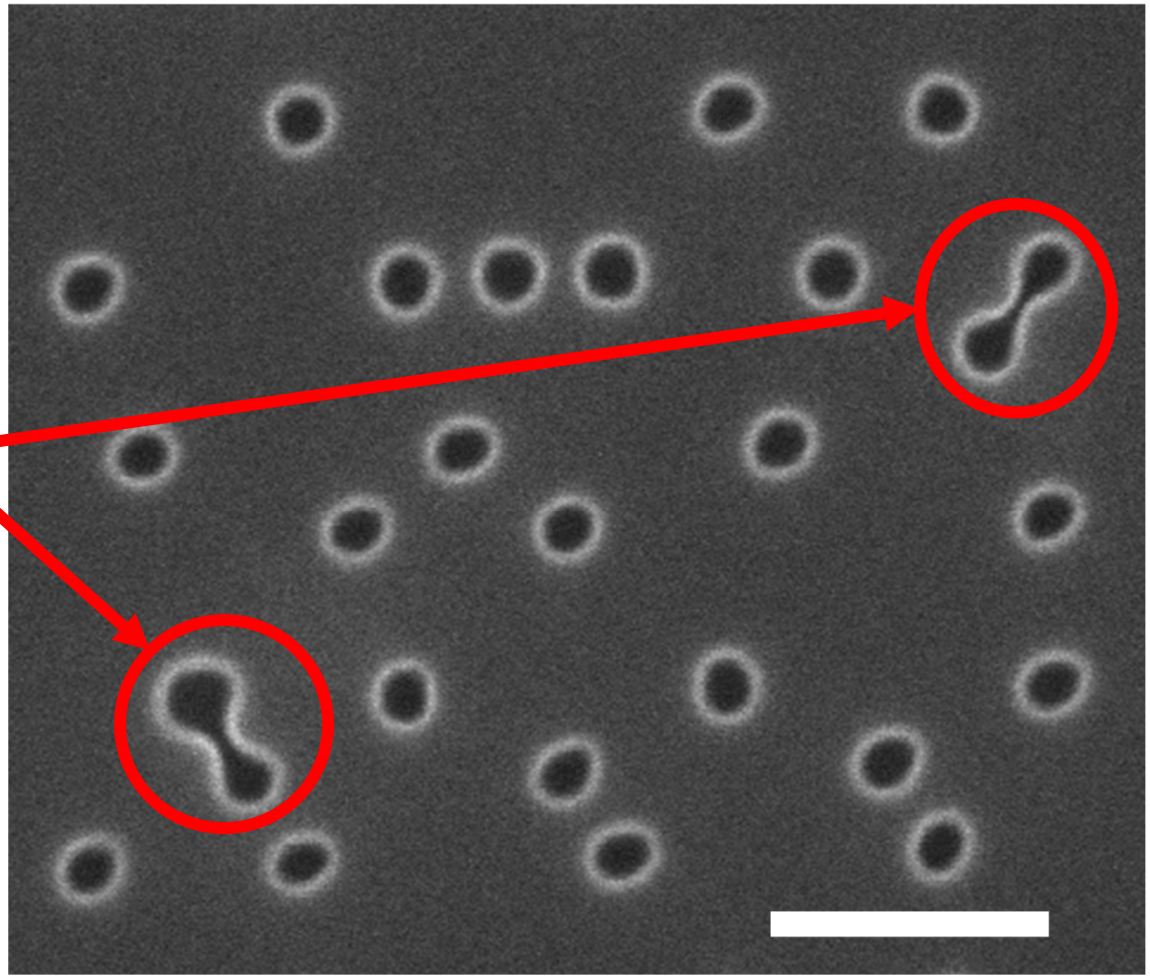
Template (SEM)

DSA results (SEM)

Scale bar: 200nm

Random Logic Circuit Patterning: 1-bit Half Adder

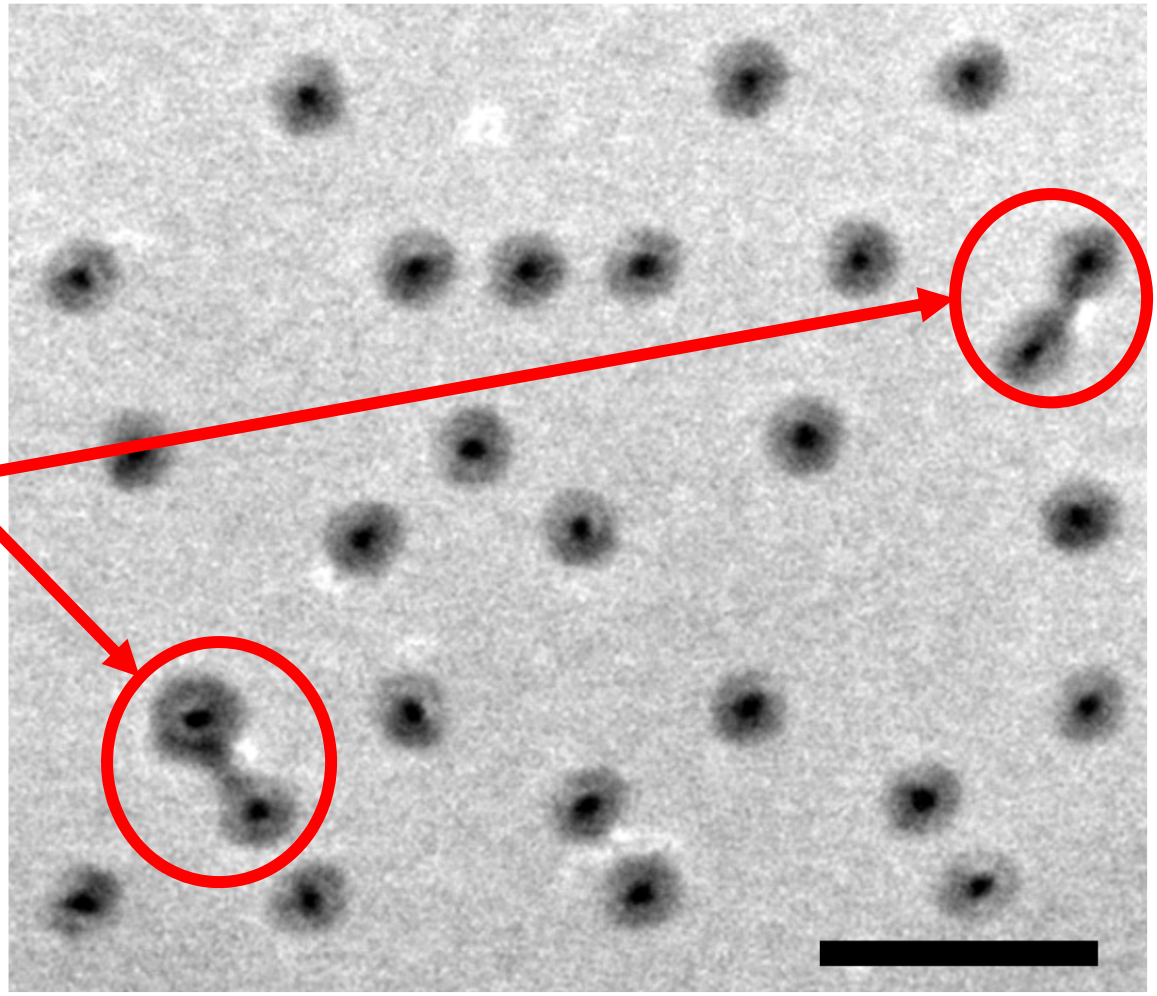
Template defects



Scale bar: 200nm

Random Logic Circuit Patterning: 1-bit Half Adder

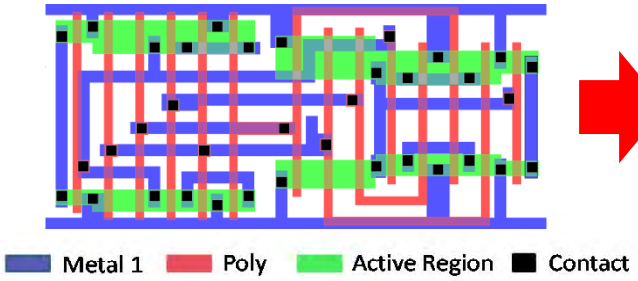
DSA heals defects



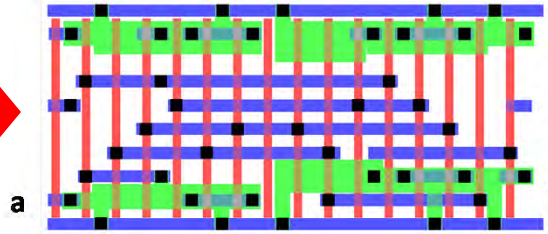
Scale bar: 200nm

Random Logic Circuit Patterning: 1-bit Full Adder

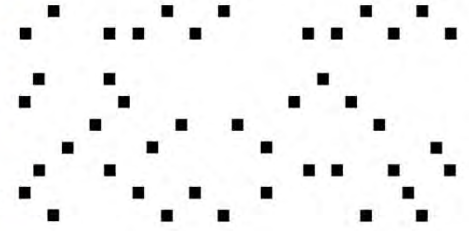
Conventional FA-X1
(Nangate 45nm Open Cell Library)



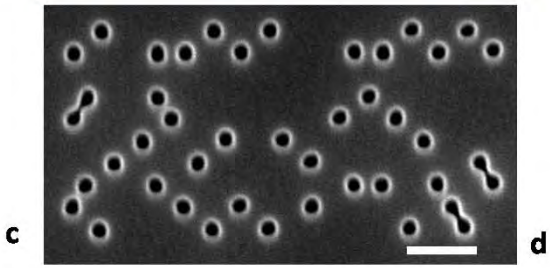
DSA-aware FA-X1

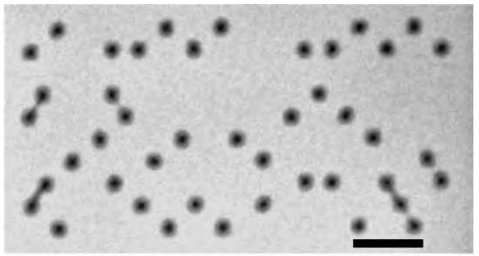


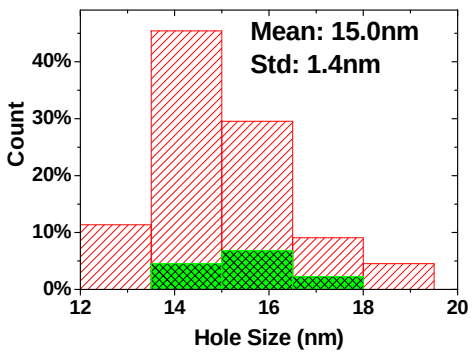
Contact Hole Layout

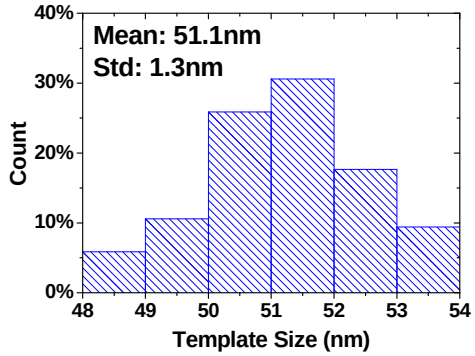


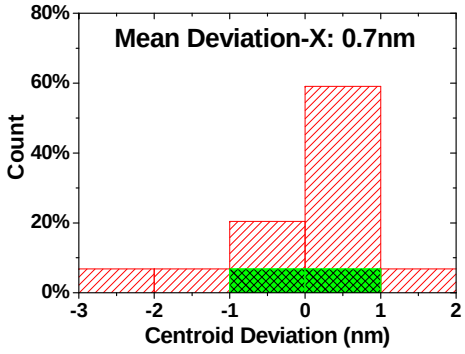
Merged templates don't affect DSA holes overlay accuracy and size variation strongly

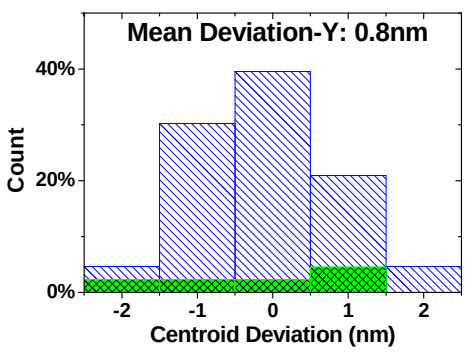








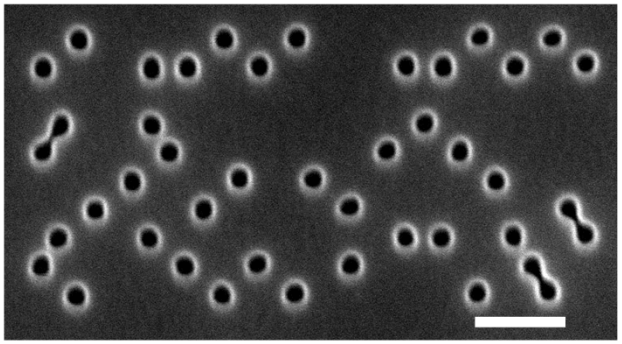


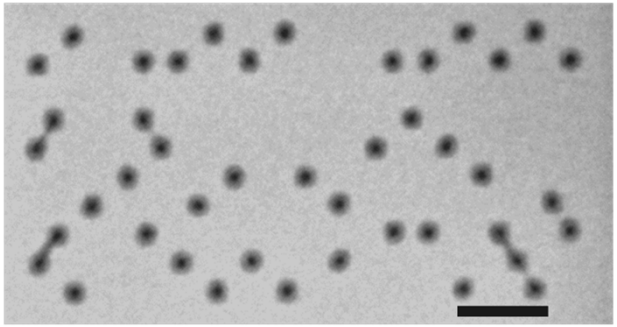


Green histogram: represent holes in merged templates.

Random Logic Circuit Patterning: 1-bit Full Adder

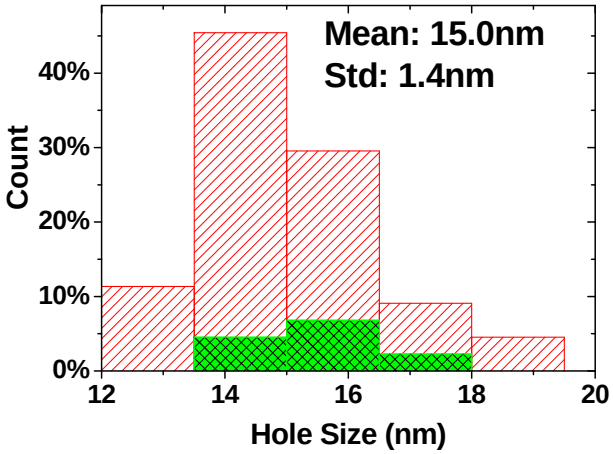
Merged templates don't affect DSA holes overlay accuracy and size variation

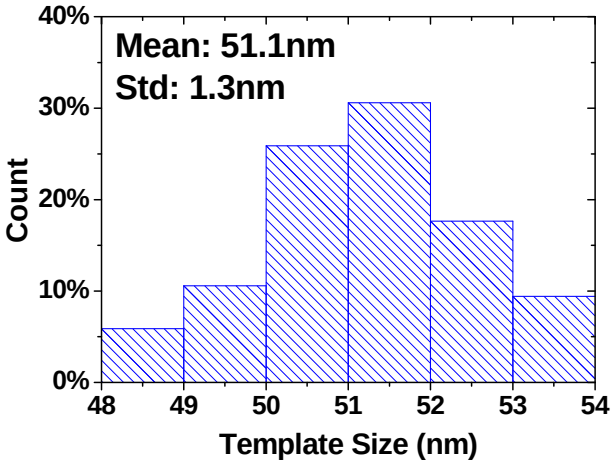


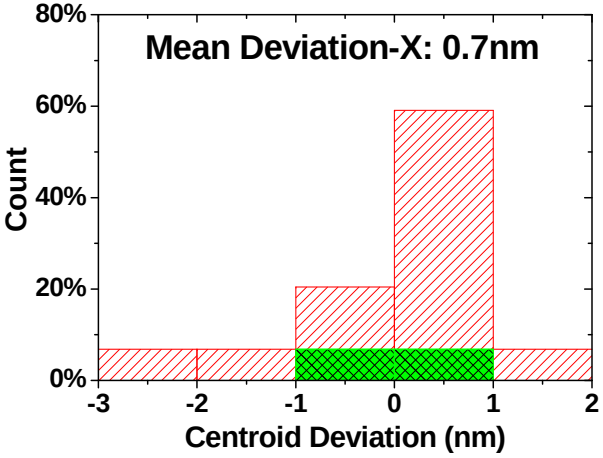


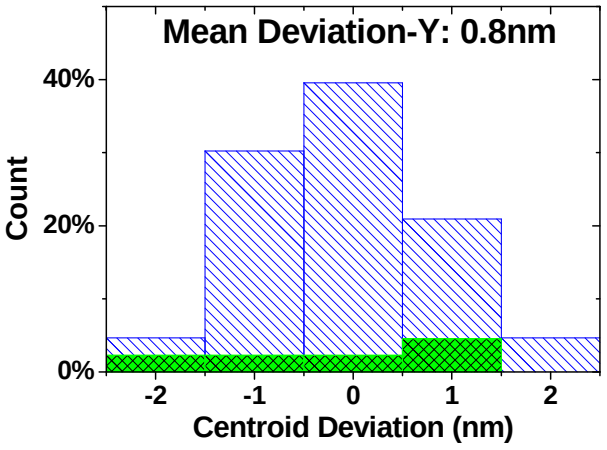
Scale bar: 200nm

Green histogram: represent holes in merged templates

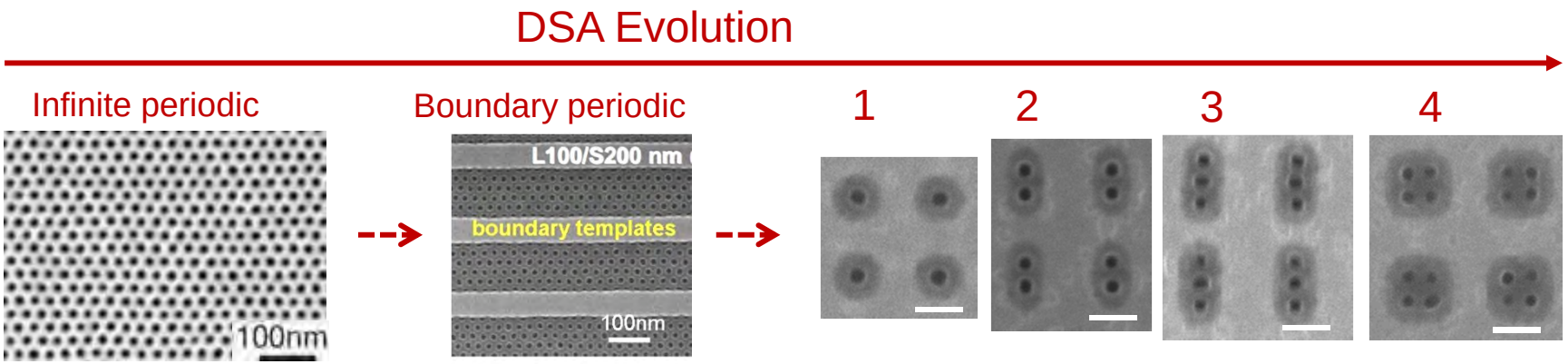








DSA for Contact Hole Patterning



193 nm immersion + DSA

=

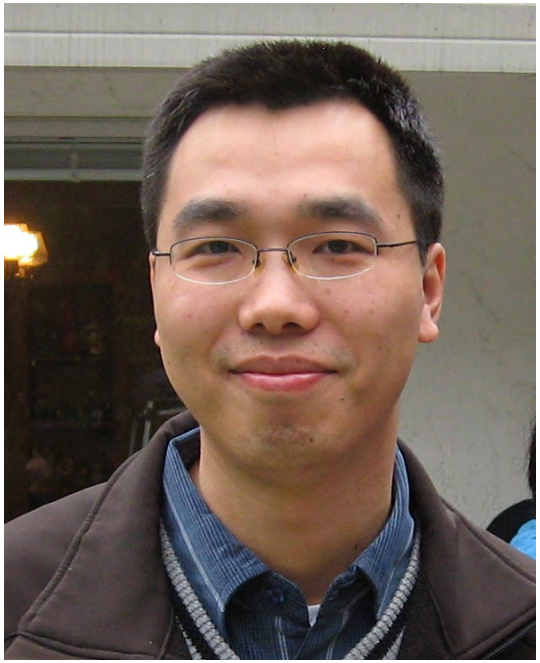
Extension of double-patterning

Looking Forward

- **Defectivity**
  - 300 mm wafer, statistical data
- **EDA tool**
  - Think OPC, DFM
  - Application of DSA must be transparent to designers
- **Develop DSA-aware template design rules**
  - Experiments, modeling

Graduated Student and Post-Doc

Li-Wen Chang
PhD 2010
Currently with Xilinx



Xinyu Bao
Post-doc (2008 – 2010)
Currently with AMAT

Collaborators

- **Applied Materials (Chris Bencher and team)**
- **Prof. Subhasish Mitra (Stanford, EE & CS Dept.)**

Sponsors and Collaborators