DPT Challenges & Litho Solutions

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Outline

- SRAM gate DPT example
  - Overlay, CDU, Resolution (Design) trade-off
- Spacer Challenges
- Litho Improvements to Enable LELE & LFLE DPT
- Conclusion
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- SRAM gate DPT example
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The Area of the SRAM cell is the most widely used Metric to determine the shrink of the node.

As a result, the area must also be used to compare Litho-DPT to Spacer-DPT shrink capabilities.

Comparison between Litho-DPT to Spacer-DPT based on 1-D geometries (1Dmetric) is not relevant.

\[ A_{SE} \text{ is a function of 3 variables } R_{SE}, OV_{SE} \text{ and } CD_{SE} \]
Process Steps Required

LELE

Spacer
Double patterning require better and more lithography

<table>
<thead>
<tr>
<th>Litho exposure equipment parameter as percentage of CD</th>
<th>Single exposure</th>
<th>Litho double patterning</th>
<th>Spacer double patterning</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔCD</td>
<td>7%</td>
<td>3.5%</td>
<td>3%</td>
</tr>
<tr>
<td>Overlay (depending on DFM)</td>
<td>20%</td>
<td>7%</td>
<td>7-20%*</td>
</tr>
<tr>
<td>#mask steps</td>
<td>1</td>
<td>2</td>
<td>2-3</td>
</tr>
<tr>
<td># process steps relative to single exposure</td>
<td>1</td>
<td>2</td>
<td>3-4</td>
</tr>
<tr>
<td>Application</td>
<td>2D, All</td>
<td>2D, All</td>
<td>1D, Mainly Memory</td>
</tr>
</tbody>
</table>

* Depending on the amount of “Design For Manufacturing” effort
OVSE and CDUSE requirements for 35nm HP SRAM (shrink of the 50nm HP SE SRAM area by 50%)

**k1 Litho-DPT**
- Below 50% line is the area of interest
- OVSE must be less than 2.5nm for 50% shrink with Litho-DPT at CDUSE=3nm
  - If current CDUSE=3nm and OVSE=5nm, a 56.2% shrink can be done with Litho-DPT

**k1 Spacer-DPT**
- Below 50% line is the area of interest
- OVSE must be less than 2.5nm for 50% shrink with Litho-DPT at CDUSE=3nm
  - If current CDUSE=3nm and OVSE=5nm, a 49.5% shrink can be done with Spacer-DPT
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Litho cost per layer: estimates for 32 nm & 22 nm
Single exposure schemes more cost effective
Spacer process can be used for random structures

**Desired layout**

**After spacer process applied**
Spacer needs overlay friendly layout to enjoy overlay advantage from the self aligned process.

- Areas surrounded by geometry formed by spacer are less sensitive to overlay errors.
- Areas not surrounded by geometry formed by spacer are more sensitive to overlay errors. Possible CD error or bridging can occur.
- Without design change, overlay is still critical for spacer when exposing a clear field mask!
Spacer with overlay friendly layout
to enjoy overlay advantage from the self aligned process

• In areas not surrounded by geometry formed by spacer, the space width between patterns must increase.
• Design change to increase the space width between patterns may need tighter overlay for next layer.
• Design change to shift a pattern to increase space width may require verification of the electrical performance.
• With these design changes, the cell size may increase.
Spacer Challenges

- CoO is higher with Spacer DPT compared to LELE/LFLE DPT
  - Spacer process integration/complexity increases cycle time

- Not all designs can benefit from Spacer DPT self-alignment
  - Burdens the designer or makes design rules overly restrictive
  - Industry not yet ready for Spacer friendly designs

- How can litho improvements mitigate the Spacer Challenges?
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Improved overlay performance options:
DCO ≤ 3.5 nm
SMO ≤ 4.0 nm
MMO ≤ 7.0 nm

Best-in-class immersion productivity (PEP & TOP options):
148 wph (300 mm)
125 x 16x32 x 30 mJ/cm²
Faster chuck swap
Faster measure cycle

Advanced lens control means improved imaging performance @ 38 nm resolution

Liquid particle counter option gives fast feedback and control of immersion water quality

iClean option boosts system cleanliness and reliability
TWINSCAN immersion overlay trend

Single machine overlay [nm]

XT:1400i (2005)

XT:1700i (2006)

XT:1900i (2007)

Next
ASML mask and system enhancements extend lithography to the limit of $k_1$

- **DoseMapper for optimum CD Uniformity**
- **GridMapper for improved Overlay**
- **Flexible off-axis & polarized illumination**
- **Application specific lens setup**
- **In-built wave-front, polarization and pupil metrology**
- **Offline Dual stage wafer height mapping**
- **Focus Dry, Expose Wet**
- **Mask enhancement techniques & optimization software**
- **Illumination source optimization & software**
Low $k_1$: High design to wafer integration

Low $k_1$ (<0.4): Integration of design, mask and lithography processes

Design For Manufacturing (DFM)

- OPC & RETs: PSM, DPT, Scatterbars, DDL verification

Application Specific Manufacturing

- Source-Mask Optimization
- Application specific tuning

Litho aware design constraints

Design space

Manufacturing space
LELE: CDU for Isolated and Dense Lines

Target CD_{litho\,1}(dense) Real CD_{litho} is smaller than target CD_{litho}

Errors caused by 1\textsuperscript{st} litho

1\textsuperscript{st} etch introduces additional $\Delta$ CD error

Overlay error: 2\textsuperscript{nd} Litho target CD \neq different from CD_{litho\,1}

Overlay error causes spaces (in a positive process) to be different

Final CD" < 10\% Target CD

Final CD includes 4 populations, two for lines, two for spaces

Dense

Iso
Litho patterning process control for CD and Overlay of 32 nm, using angle-resolved scatterometry

Raw etched poly CDU

Mean CD

Overlay between litho 1 and 2

< 4.9 nm

< 7.0 nm

< 6.3 nm

99.7% OVL X = 4.0 nm
99.7% OVL Y = 4.2 nm

< 2.8 nm

< 3.8 nm

< 0.8 nm

99.7% OVL X = 3.2 nm
99.7% OVL Y = 3.4 nm

Jo Finders et al. | SPIE San Jose, Feb 26, Ref. 6924-07
“Double patterning for 32 nm and below, an update”
LFLE: CDU for Isolated and Dense Lines

**Wafer does not leave litho cluster**

Real CD\(_{\text{litho}}\) is smaller than target CD\(_{\text{litho}}\)

Errors caused by 1\(^{\text{st}}\) litho

Track freeze process introduces additional ∆ CD error

Overlay error causes spaces (in a positive process) to be different

2\(^{\text{nd}}\) Litho: target CD ≠ different from CD\(_{\text{litho}}\)

“Final CD” < 10% Target CD

Final CD includes 4 populations, two for lines, two for spaces
Litho double patterning process (LFLE) control for CD & Overlay of 32 nm: wafer did not leave the litho cell

Line 1
Mean = 33.5
3σ = 2.8 nm

Line 2
Mean = 37.5
3σ = 1.3 nm

Space 1
Mean = 29.1
3σ = 3.3 nm

Space 2
Mean = 27.8
3σ = 2.7 nm

Litho 1
NA = 1.0
Dipole illumination
σ₀/σᵢ = 0.86/0.65

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Litho double patterning process (LFLE) control for CD & Overlay of 32 nm: wafer did not leave the litho cell

\[ DPT_{OL} = P - P_1 \]

\[ P_1 = \frac{P_{1L} + P_{1R}}{2} \]

Overlay

\[
\begin{array}{c}
\text{Mean:} & 0.71 \\
3 \text{ Sigma:} & 2.38 \\
\text{Max:} & 3.29 \\
99.7\%: & 3.19 \\
\text{Nr. of points:} & 331 \\
\text{Nr. of flyers:} & 53
\end{array}
\]

DPT overlay \(3\sigma < 2.5\text{nm}\)
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Conclusions

- **Spacer Challenges**
  - Not all designs can benefit from Spacer DPT self-alignment
  - Burdens the designer or makes design rules overly restrictive
  - Additional cost/complexity (cycle time) serves as a detractor

- **Litho Challenges/Improvements**
  - Spacer, LELE & LFLE require much tighter CDU than required from SE lithography; LELE/LFLE must also achieve overlay on the order 3nm
  - Intra-layer overlay not as challenging as inter-layer overlay due to elimination of some process effects.
  - Tighter CDU and overlay budgets should be achieved through active compensation of wafer and field spatial distributions
  - DoseMapper to reduce intra-field and inter-field CDU due to reticle, track, and etch CD variation
  - GridMapper to reduce intra-field and inter-field OV due to reticle registration and wafer distortion

- **XT:1950Hi drives performance improvements to further enable DPT processing.**

- **Future improvements planned in productivity, overlay & imaging to enable cost effective lowk1 solutions.**
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