Self-Aligned Double Patterning for 3xnm Flash Production

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think it. apply it.™

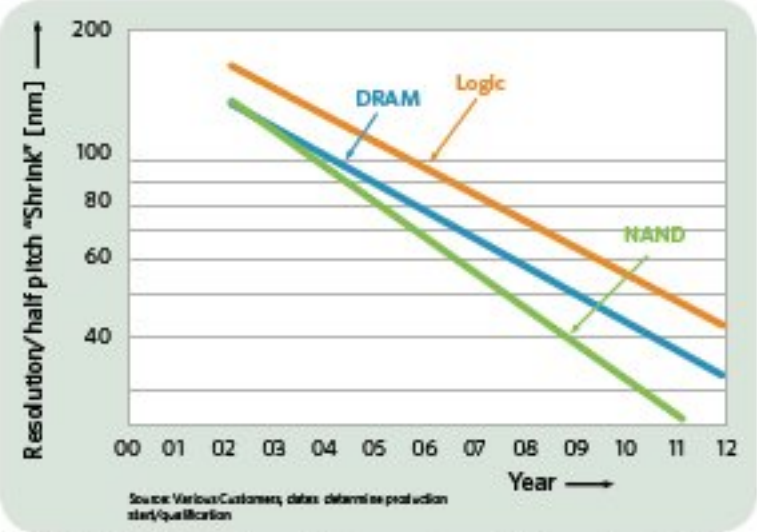
Overview

- Double Patterning Drivers for Flash
- Comparison of Double Patterning Schemes
- Applied Materials Self-aligned Double Patterning (SADP)
  - SADP Approach & 32nm Demonstration
  - SADP 22nm Extendibility
  - Application Demonstration
  - Production Proven Products for SADP Flash Manufacturers
- Summary

Double Patterning Drivers

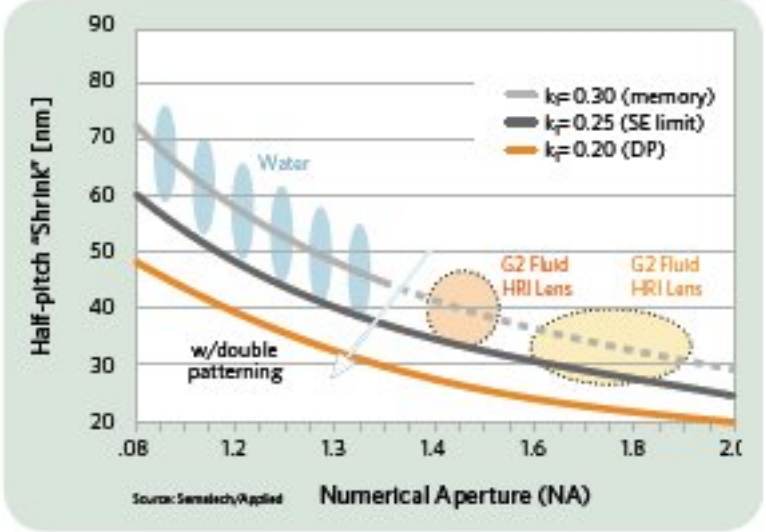
Drivers for SADP

NAND FLASH DRIVES LITHO SCALING



NAND Flash is driving the resolution requirements below 45nm by 2008. DRAM will follow one to two years later.

RESOLUTION BARRIER FOR SINGLE EXPOSURE



With 193nm exposure wavelength and current NA, double patterning is the only way to reach the required half-pitch for 32nm.

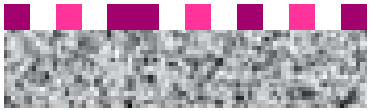
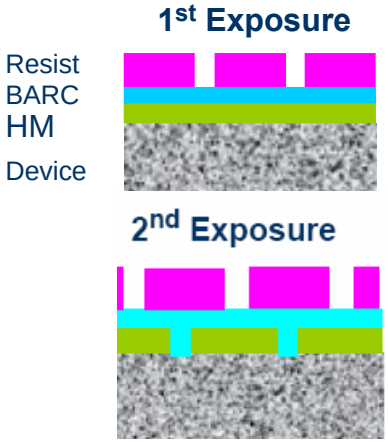
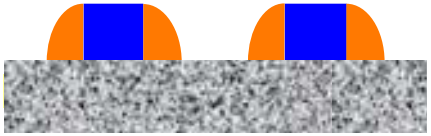
Flash - Aggressive half pitch needs

Immersion Lithography – Resolution limitations

Self-aligned double patterning (SADP) provides the capability to achieve aggressive half pitch at relaxed litho conditions

Double Patterning Schemes

Double Patterning Approaches

Type	Double Imaging	Double Patterning	Self Aligned Double Patterning
Process Flow	 ▪Coat Expose Develop ▪Resist Freeze ▪Coat Expose Develop		 ▪**One critical exposure** ▪Spacer Technology
Overlay (Requirement: <3nm)	~ 6-8nm	~ 6-8nm	not applicable
CDU (Requirement: <3-4nm)	Line - 2nm Space – 3.7nm (w/o Overlay) Space – 5.1nm1 (w/ Overlay)	Line - 2nm Space – 3.75nm (w/o Overlay)	Line < 1.5nm Space < 3.0nm (1 population combining S1 & ,S2)
Line Edge Roughness (Requirement: <3-4nm	~ 4-5nm	~ 3-4nm	< 2nm (Applied process)

SADP Scheme Comparisons

Process Scheme / Metrics	 **Negative Line by Fill Poly Core**	 **Positive Line by Spacer Resist or SOH Core**	 **Positive Line by Spacer APF Core**
CDU, 3σ Line/Core/Gap	Good for trench	Good for line	Good for line 1.1 / 1.7 / 2.4nm
LER	Poly ~3.5nm	Same as PR	<2nm
Core Mech Integrity	Good	Poor	Good
Materials Selection	Thermal budget, gapfill, spacer SC	New Materials for PR and Spacer, thermal budget	Known films (APF, PE Spacer)
Defectivity	High (Poly Etchback)	Low	Low (Defect gallery in dev)
Extendibility to 2xnm	Gapfill issue	PR height & integrity	Demonstrated to 2x

SADP: Memory Makers' Production Choice

Samsung touts 30nm NAND flash using self-aligned double-patterning

Solid State Technology

October 23, 2007 - Samsung Electronics Co. Ltd. says it has developed 64Gb multilevel cell NAND flash memory chip using 30nm process technology, built using double-patterning lithography, with commercial chips ready in about a year.

The new device utilizes a process called "self-aligned double patterning technology" (SaDPT), an upgrade from charge trap flash that Samsung has used for NAND flash on silicon nitride. in SaDPT, the first pattern transfer is a wider-spaced circuit design of the target process technology, then a second pattern transfer fills in the spaced area with a more closely designed pattern (see figure).

Samsung says it will use SaDPT with "existing photolithography equipment" for production using the 30nm process technology, targeting commercial production in 2009. In addition to the 64Gb MLC device, it has also built a 32Gb single-level cell NAND flash chip. Up to 16 64Gb flash devices can be combined into a 128GB [illegible] MP3 music files, the compa

Top Story: Lithography is among top productivity challenges

Semiconductor International

November 8, 2007 -- Lithography is among the top productivity challenges facing the semiconductor industry, but packaging and testing costs are another area that must be addressed, according to Jin Seog Choi, chief technology officer at Hynix Semiconductor Inc. (Icheon, South Korea).

In a panel presentation at the International Trade Partners Conference (ITPC), held this week in Maui, Hawaii, Choi addressed the future technologies needed to keep cost reductions on track.

Starting in 2009, when NAND devices are using 30-35 nm design rules and DRAM is in the 43-48 nm range, the memory manufacturers face critical lithography choices. Extreme ultraviolet (EUV) lithography offers a low k1 factor, but it is unclear when EUV will be ready for high-volume manufacturing. **Spacer patterning technology could be used for NAND memories** or double patterning lithography may be required, for both DRAM and NAND devices.

However, double patterning "has a high cost of ownership. The low throughput of double patterning is a key issue," Choi said…

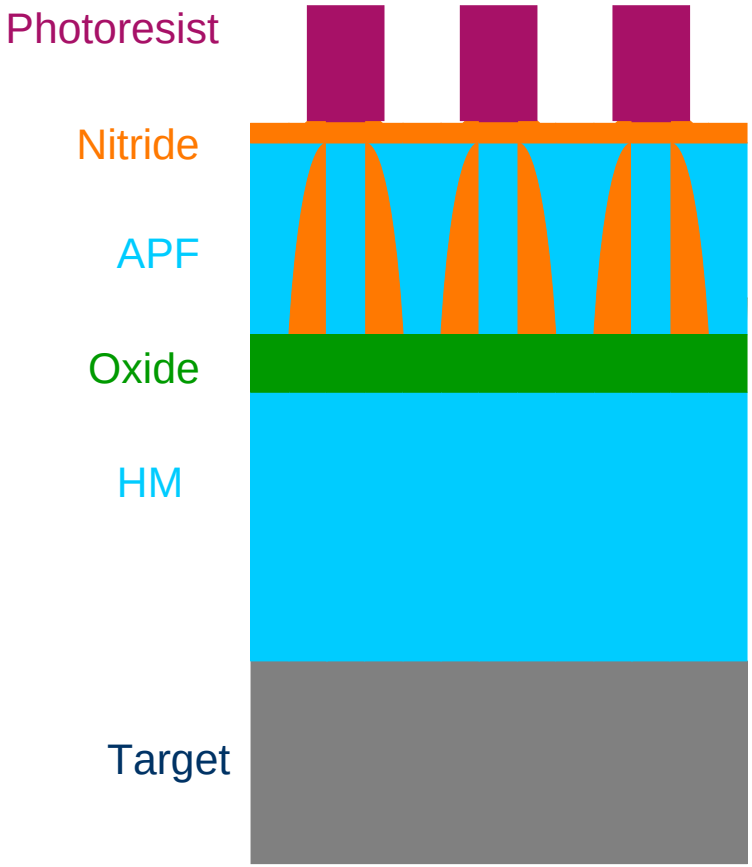
Major NAND Flash Manufacturers have adopted SADP scheme as the baseline for 3xnm critical layers module development

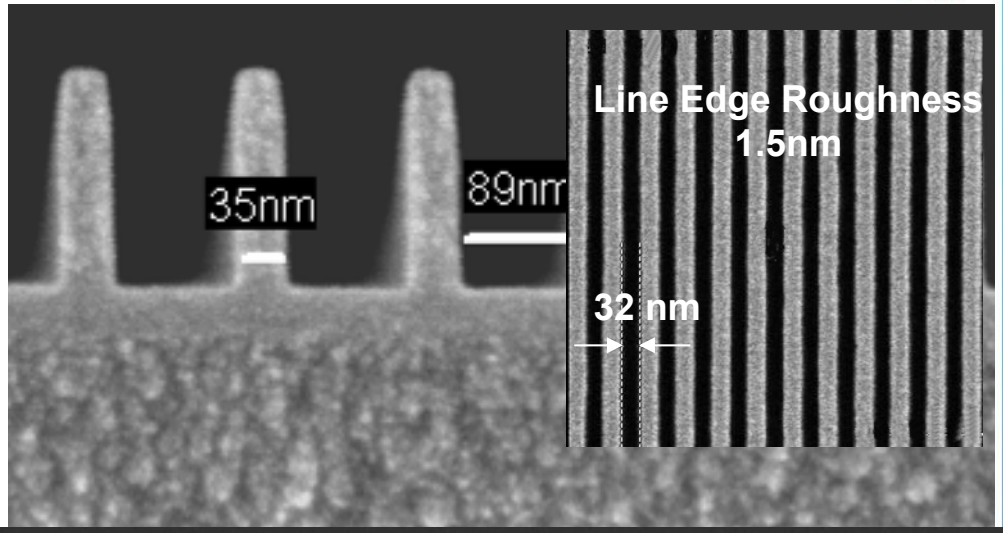
32nm and 22nm APF based SADP

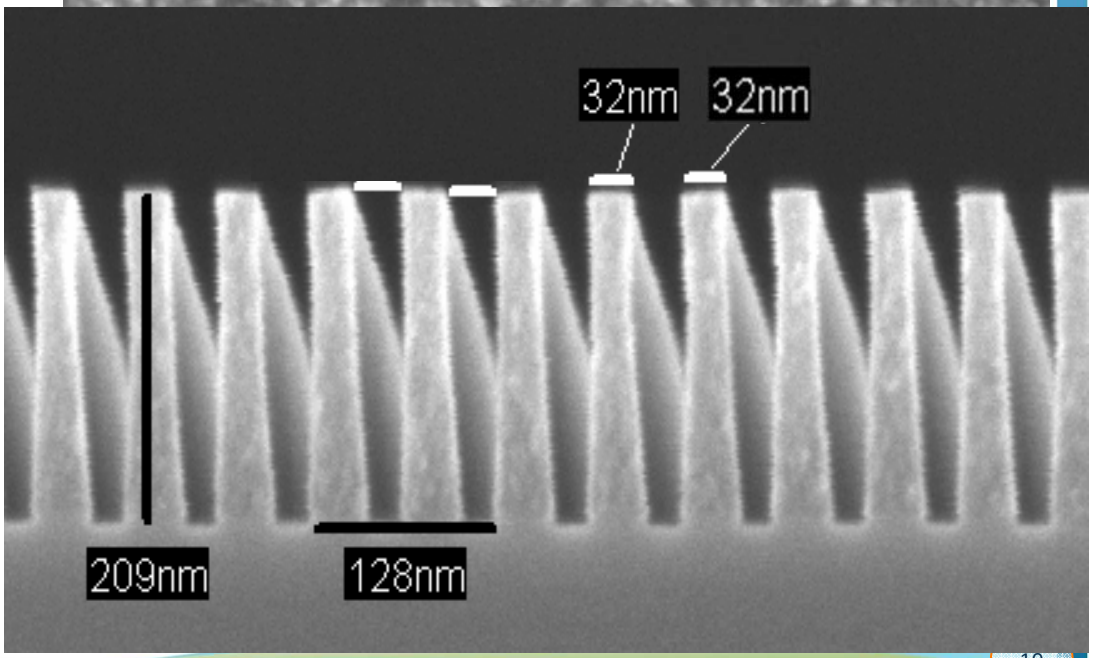
APF Properties: Integrity, Alignment
SADP Scheme Performance, LER
CDU: Line vs Space

Self Aligned Double Patterning Scheme

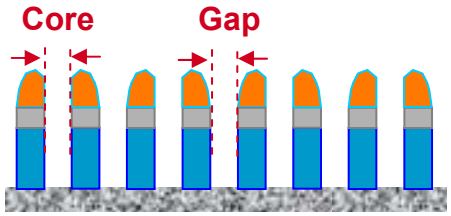
Print 32nm L&S with 193 dry



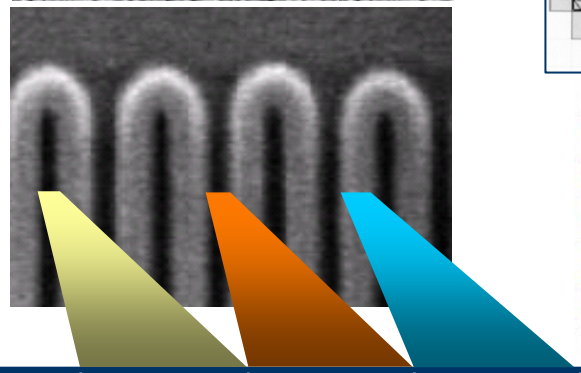




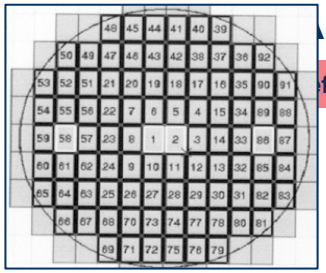
AMAT 3X SADP Performance Summary

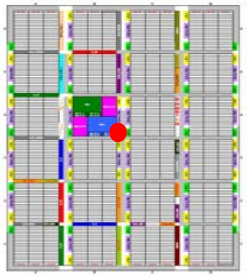


Top-view
(Illustrative)

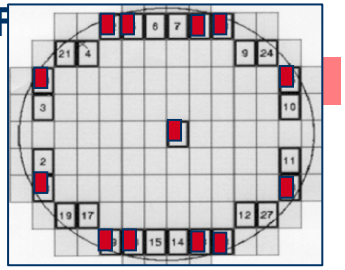


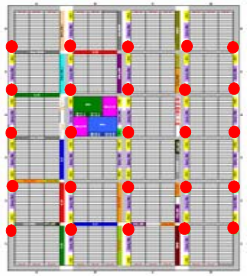
Map 1: 92 Die
1 point per die



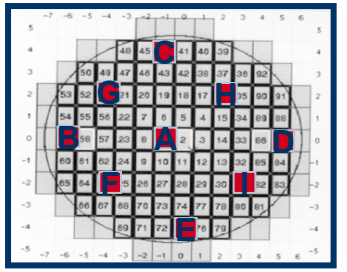


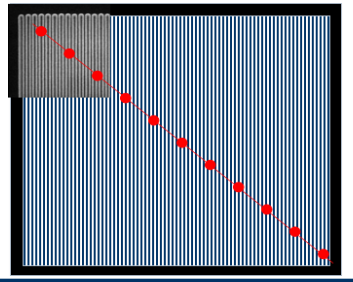
Map 2: 4 full die, 8 partial
25 sub-die locations





Map 3: 9 die
11 locations across array





	Core (nm)	Gap (nm)	Line (nm)	Core-Gap Delta (nm)	LER (nm)	LWR (nm)	Core CDU 3σ (nm)	Gap CDU 3σ (nm)	Line CDU 3σ (nm)
92 die 1 pt	26.4	26.5	38.1	0.1	1.4	1.5	3.1	2.7	1.1
Wafer Edge	27.1	25.7	38.2	-1.4	1.4	1.3	2.5	3.2	1.4
Within Array			39.0		1.7	1.9			0.9

- 0.1nm CD difference between core & gap
- CDU <2.4nm
- Litho LWR 3.5nm → Bottom APF LWR 1.4nm

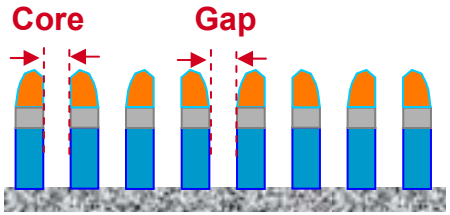
APF

AdvantEdge G5 Etch

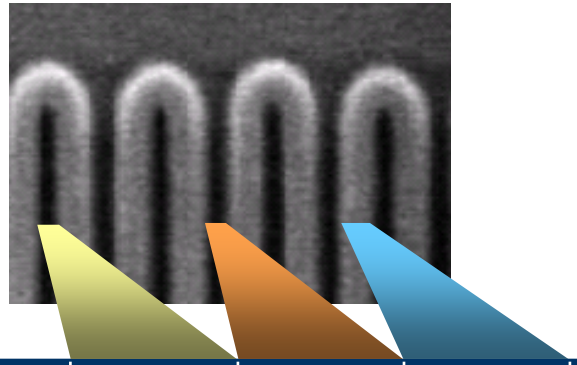
NDP Spacer

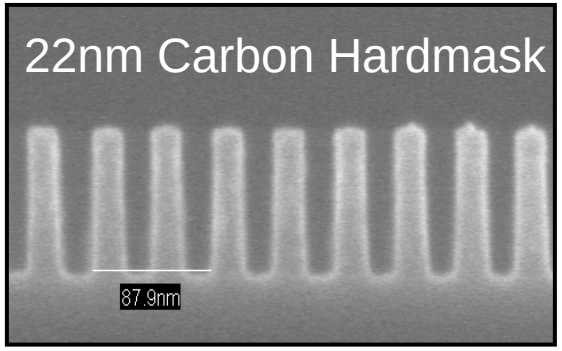
22nm Extendibility

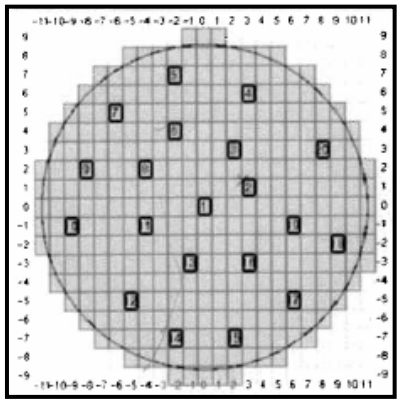
Summary of AMAT 22nm Spacer Mask Demonstrations:



Top-view







*Results from 20 die measurement

		Immersion Litho	Core	Gap	Line	LER Core	LER Gap
Mean (nm)	Slot 16	47.6	24.1	22.9	22.8	1.6 nm	1.7 nm
	Slot 25	47.5	24.7	22.7	22.5	1.6 nm	1.5 nm
3σ (nm)	Slot 16	1.8	1.7	2.2	1.8		
	Slot 25	1.8	2.0	2.5	1.1		

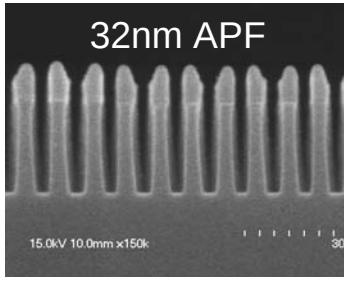
Demonstrated extendibility to 22nm

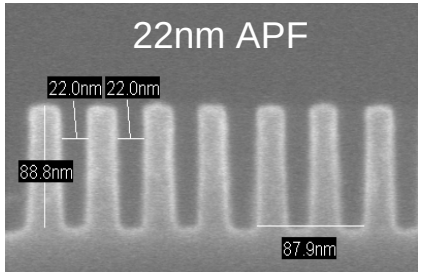
- CD Control of 2nm (3σ)
- LER <2nm

Application Demonstration

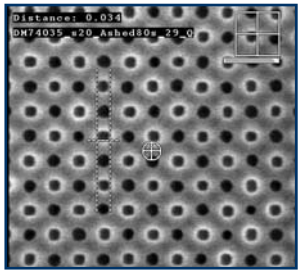
Applied Materials SADP Demonstrations

Demonstrated Hardmask Patterning

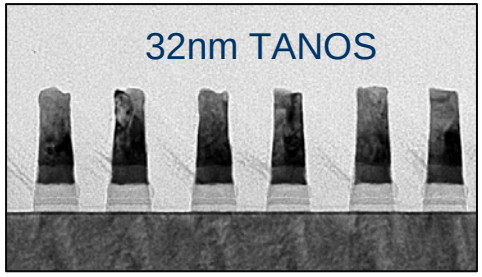


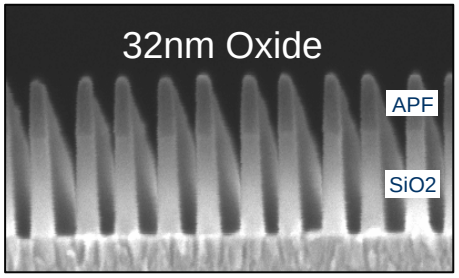


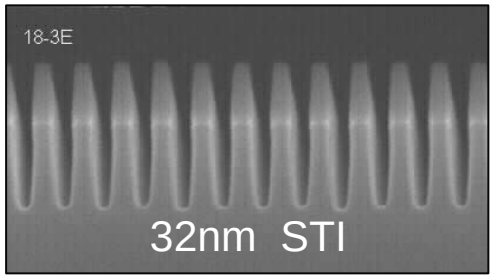
34nm Self Aligned Dense Contact HM

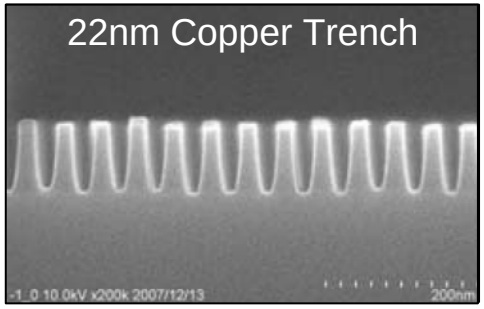


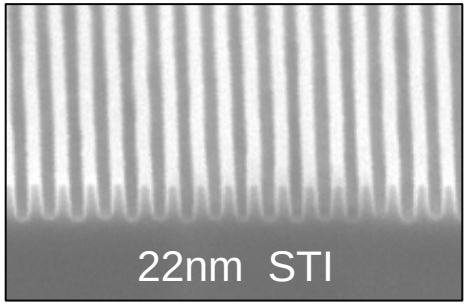
Demonstrated Applications:

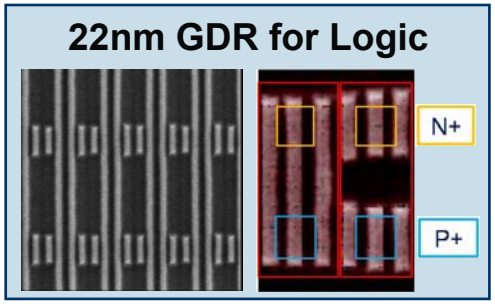










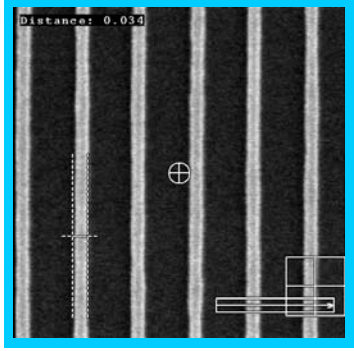


Demonstrated on Flash critical dimension applications

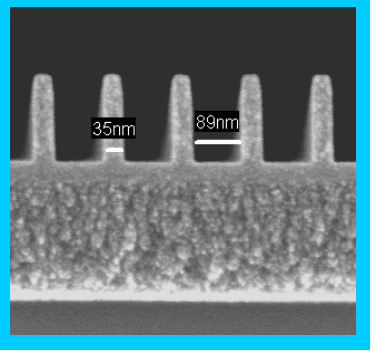
32nm SADP Process Flow for TANOS Flash

SADP Etch 1 Process

CD Trim

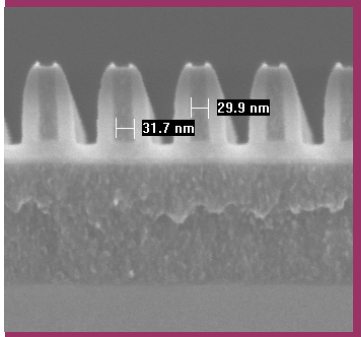


Top APF Etch

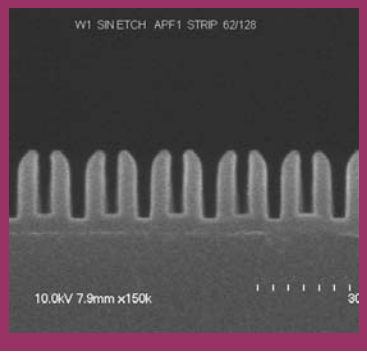


SADP Etch 2 Process

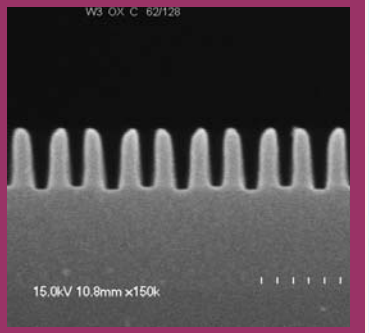
Spacer Etch



APF Strip-Out

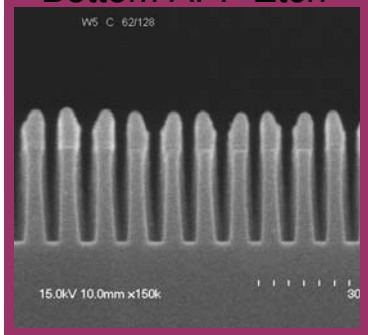


Etch Stop Etch



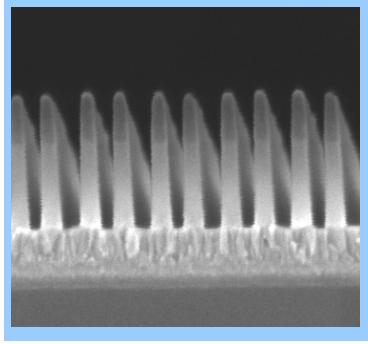
SADP Etch 2 Process

Bottom APF Etch

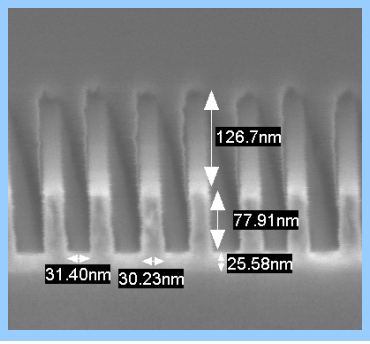


Metal Gate Etch Process

Oxide H.M. Etch

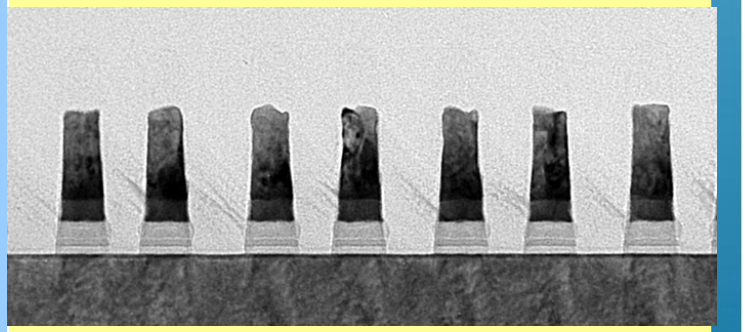


W / WN / TaN



HiK Etch Process

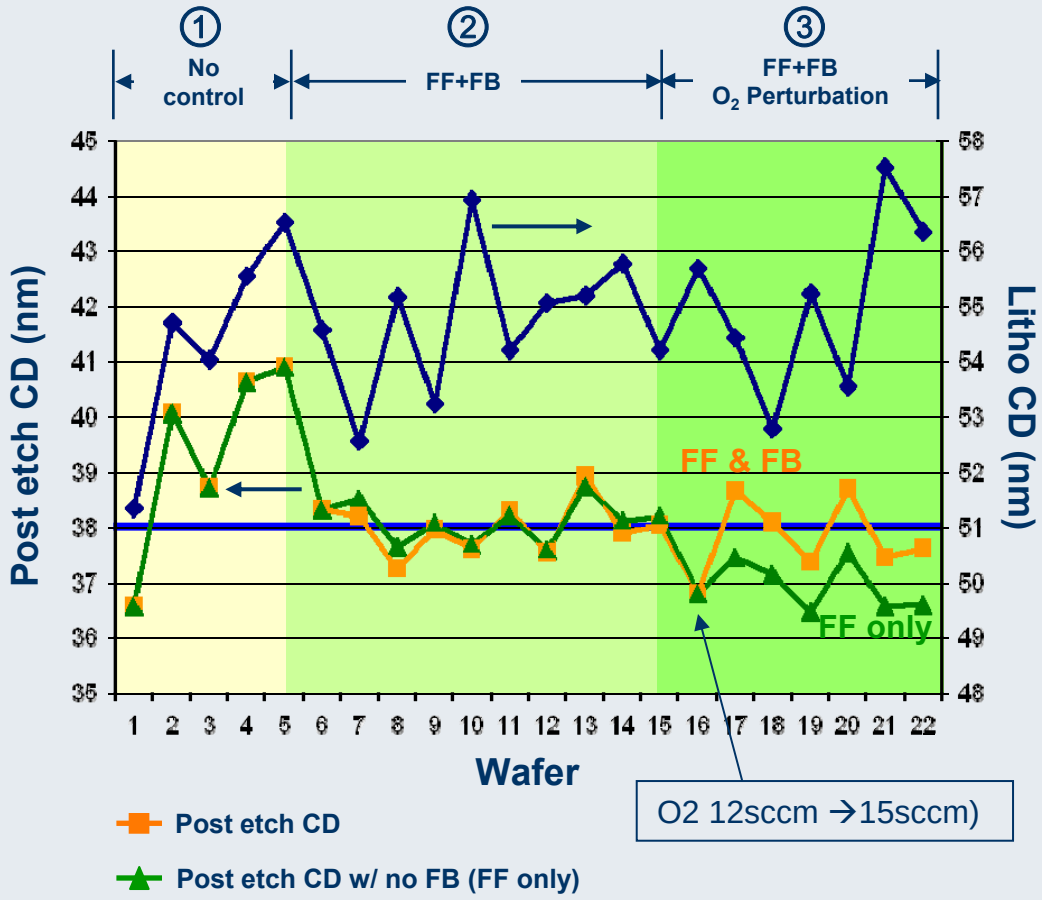
Al2O3 and Si3N4



- AMAT AdvantEdge etch chamber was used for all patterning etch steps
- SADP only required 2 etch steps for patterning

Core APF Automatic Process Control (APC) on G5

FF and FB Control (Litho -> Trimming/BARC/APF Core Etch)



- wafers were generated with an intentional CD variation to demonstrate FF and FB capability
  - Litho CD Range 6.2nm and CD 1σ: 1.49nm
  - Target CD is 38nm.
- Wafers were split into three groups:
- Group 2 and 3:
  - Incoming CD 1σ: 1.38nm
  - Post etch CD 1σ: 0.57nm

Demonstrated WTW CD control of 1.5% of target CD, despite intentional incoming CD variation and O_2 flow perturbation.

AMAT SADP Products

AMAT is ready for patterning 32nm & beyond

- Technologies available on proven manufacturing platforms to reduce risk and time to market

Producer® APF™ NDP™ PECVD

AdvantEdge™ G5 Etch

UVision® SP Brightfield

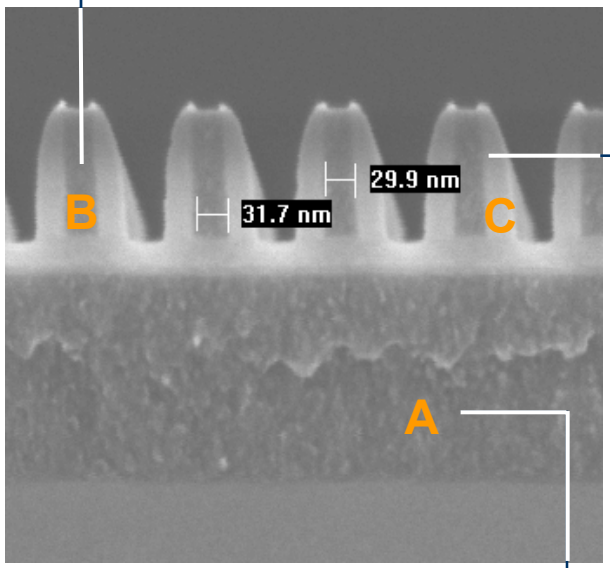
VeritySEM™ Metrology

- Demonstrated Spacer Self-Align Double Patterning
  - 32nm Lines & Spaces with TANOS Stack, STI, oxide
  - 22nm Lines & Spaces with oxide & gridded STI structures
  - Achieved:
    - **LER [<1.7nm]**
    - **CD Uniformity [<2nm]**
    - **Overlay [<3nm]**

SADP is ready today for 32nm production
Extendibility to 22nm is proven

Summary

SADP: Spacer Mask Approach



APF Core
- Good LER
- Ashable – no wet clean required
- Stable at high temp - spacer temp requirement relaxed as a result

NDP Spacer
- >80% step coverage
- Good uniformity
- Good long range micro-loading performance

G5 for all SADP etch steps
- All-in-one chamber for all SADP etch steps & pattern etch
- Good CDU
- High productivity – no warmup necessary

APF Hardmask
- Good LER of 2nm
- Good line bending resistance
  5:1 at 32nm; 4:1 at 22nm

Full Portfolio Of Products Available For SADP Integration Schemes - Including UVision for defect analysis and Verity for CD measurement

think it. apply it.™

APPLIED MATERIALS®