IDeAL program: DSA activity at LETI

S. Tedesco - R. Tiron - L. Pain
Outline

- The IDeAL program
- Graphoepitaxy of BCP
- Contact hole application
- 300 mm pilot line in LETI
- Conclusion
Why DSA for Microelectronics?

- Block copolymers self assembly capabilities
  - Very high resolution
  - Low intrinsic Line Edge Roughness
  - Easy process
  - Low cost

- C-MOS Lithography constraints
  - Control the domain orientations (1D - 2D)
  - Alignment control with respect to a preview level
  - Integration capabilities
  - Low defectivity
  - Respect of design rules
Why DSA for Microelectronics?

Advanced lithography SPIE conferences

- DSA a complementary lithography techniques that could get inserted as early as the 14nm node
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LETI DSA open program

Insertion of Directed self Assembly Lithography
Directed Self Assembly: the Lithography?

- **Objectives**
  - A new open program to develop a full DSA solution
  - Joint work in LETI environment on material, processes, demonstration & integration
  - A cluster open to materials and equipments’ suppliers, IDM, EDA

- **Partnership status – July 2012**
  - DSA material development
    - Copolymer material worldwide leader:
    - Collaboration with academic laboratories
    - Resist partners: under progress
  - Equipment suppliers
    - 2 industrial partners
  - End users
    - Bilateral work with
Arkema in a few points

- Worldwide player in specialties chemistry
- Ranging from 1st to 3rd position in product lines insuring 80% of the company revenue.
- 2010 revenue: 5,9 Md€
- R&D: > 120M€ / 8 R&D center WW (US, Japan, France)
- Annual Capex: 293 M€
- 80 industrial sites
- 15 000 employees

ARKEMA strength:
- Worldwide polymer manufacturer
- Strong know-how on block copolymer
- Ability to quickly ramp-up from R&D to industrial scale
missions?

- Push material platforms to maturity
  - From lab scale to industry
  - Evaluate advanced copolymer platform

- Develop 300mm patterning solutions
  - Certify material compatibility with clean room standard
  - Screen DSA material performances
  - Verify transfer capabilities

- Scale-up DSA processes to production level
  - Compatibility with design rules
  - Respect of ITRS standard: defectivity, throughput...
How to go from R&D to industrial?

A production-oriented consortium

DSA Materials

Scale-up material qualification

Industrial scalability

Pre-industrial reactor

Lab. scale

Integration

300 mm INTEGRATION
– Defectivity
– Design compatibility

Process development

First 300 mm demonstration
– Process development
– Etch, Strip, …

Samples:
– Material compatibility
– Material properties

Process capability
– Throughput
– Patterning capability

Maturity III

Maturity II

Maturity I

Industrialization

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ARKEMA – LETI partnership: materials path

- Efficient neutralization layer
- Several materials under screening
  - PS-PMMA platform
  - High $\chi$ platform

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**PS-b-PMMA BCP**

CD $\approx$ 15nm

**High $\chi$ BCP**

CD = 7nm

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Why grapho-epitaxy preference?
A versatile process
LETI demonstration
How to find optimum guiding litho process?

=> Influence of Litho1 design rules & BCP material

Design rule compatibility

Zero Defect Configuration

Before litho1 optimization

After litho1 optimization

Defectivity measurement enables lithography and process optimization
Silicon Etching with Copolymer Lithography

Initial mask (PS) 30 to 100 nm thick

SiO₂ Mask (10 nm)

- Brush opening (Ar/O₂ plasma)
- PS plasma treatment
- Mask etching (CF₄ based plasma)
- Silicon etching (HBr/Cl₂/O₂ plasma)

Copolymer etching process fully compatible with CMOS requirements

“Self-assembly patterning using block copolymer for advanced CMOS technology: optimisation of plasma etching process”
Thierry Chevolleau, CNRS (France)- Paper 8328-20, SPIE2012
Silicon Etching with Copolymer Lithography

Copolymer etching process fully compatible with CMOS requirements
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Contact shrink and multiplication using DSA of BCP

Integration (litho+etch) demonstrated for contact shrink and multiplication
How to define design rules: Example of code

- Design
- Calculated CH placement

Simulation contour

Contour variation w.r.t. dose, focus and mask CD error variations

Experimental validation

53nm

Extracted Contour
Calculated CH position
CH position on wafer
Outline

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### DSA 300 mm infrastructure on SOKUDO RF³ track

#### Process steps

<table>
<thead>
<tr>
<th>Process steps</th>
<th>CMOS requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Guided litho</td>
<td>➢ Resist hardness to bake and solvent</td>
</tr>
<tr>
<td>PS-r-PMMA spin coat.</td>
<td>➢ metal/ ionic contamination ➢ solvent compatibility</td>
</tr>
<tr>
<td>Grafting</td>
<td>➢ Bake time and temp.</td>
</tr>
<tr>
<td>Rinse</td>
<td>➢ solvent compatibility</td>
</tr>
<tr>
<td>Copolymer coating</td>
<td>➢ metal/ ionic contamination ➢ solvent compatibility</td>
</tr>
<tr>
<td>Self assembly</td>
<td>➢ Throughput ➢ Defectivity</td>
</tr>
<tr>
<td>Etching</td>
<td>➢ Transfer capabilities</td>
</tr>
</tbody>
</table>

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“Pattern density multiplication by direct self-assembly of block copolymers: toward 300mm CMOS requirements”  
Ralucă Tiron et al, CEA-Leti (France) - Paper 8324-23, SPIE2012

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Front-end production  
300mm track & scanner
Shrink of contact holes 300mm process

graphoepitaxy with standard lithography 193nm

CD ~ 100nm

CD ~ 15nm
Shrink of contact holes 300mm process
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To conclude

- DSA a complementary lithography technique that could get inserted as early as the 14nm node
  - In a first step by using PS-b-PMMA like materials
  - In a second step by using high $\chi$ materials

- A realistic application: contact hole shrink and doubling

- Defectivity is key

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