


IDeAL program : DSA activity at LETI

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Outline

- 
- The IDeAL program
 - Graphoepitaxy of BCP
 - Contact hole application
 - 300 mm pilot line in LETI
 - Conclusion



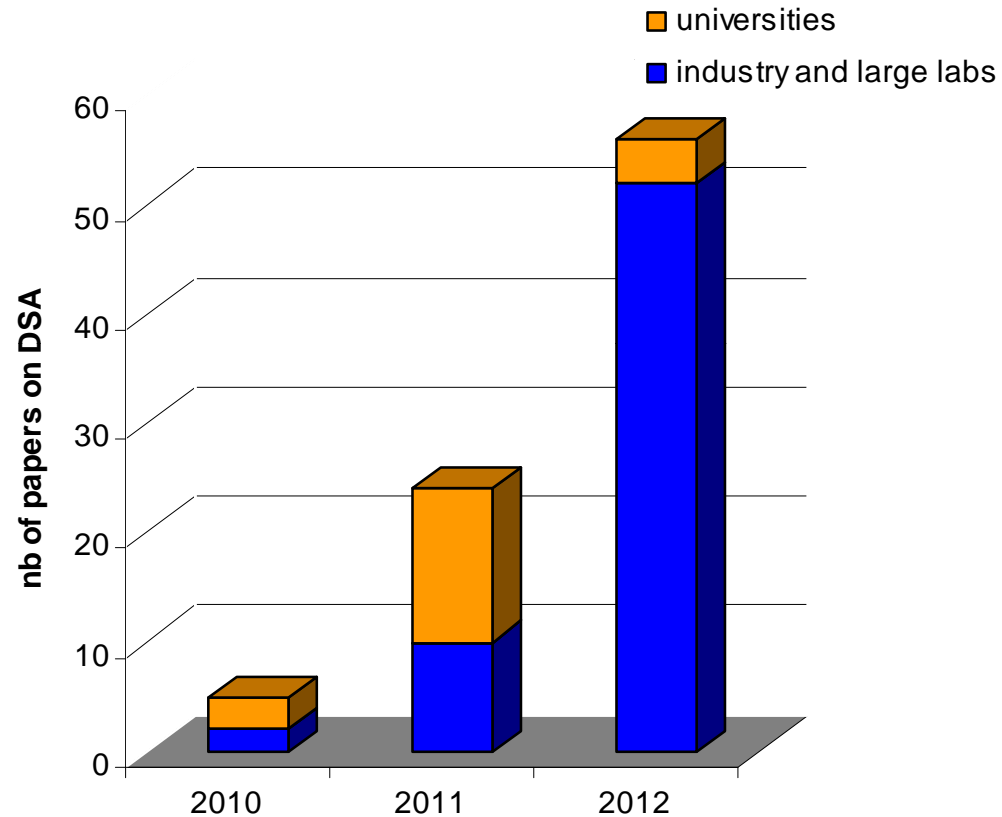
Why DSA for Microelectronics ?

- Block copolymers self assembly capabilities
 - Very high resolution
 - Low intrinsic Line Edge Roughness
 - Easy process
 - Low cost
- C-MOS Lithography constraints
 - Control the domain orientations (1D - 2D)
 - Alignment control with respect to a preview level
 - Integration capabilities
 - Low defectivity
 - Respect of design rules



Why DSA for Microelectronics ?

Advanced lithography SPIE conferences



DSA a complementary lithography techniques that could get inserted as early as the 14nm node



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LETI DSA open program



Insertion of Directed self Assembly Lithography



Directed Self Assembly : the lithography?

■ Objectives

- A new open program to develop a full DSA solution
- Joint work in LETI environment on material, processes, demonstration & integration
- A cluster open to materials and equipments' suppliers, IDM, EDA

■ Partnership status – July 2012

- DSA material development
 - Copolymer material worldwide leader :
 - Collaboration with academic laboratories
 - resist partners : under progress
- Equipment suppliers
 - 2 industrial partners
- End users
 - Bilateral work with



Arkema in a few points

- Worldwide player in specialties chemistry
- Ranging from 1st to 3rd position in product lines insuring 80% of the company revenue.
- 2010 revenue : 5,9 Md€
- R&D : > 120M€ / 8 R&D center WW (US, Japan, France)
- Annual Capex : 293 M€
- 80 industrial sites
- 15 000 employees

ARKEMA strength :

- Worldwide polymer manufacturer
- Strong know-how on block copolymer
- Ability to quickly ramp-up from R&D to industrial scale





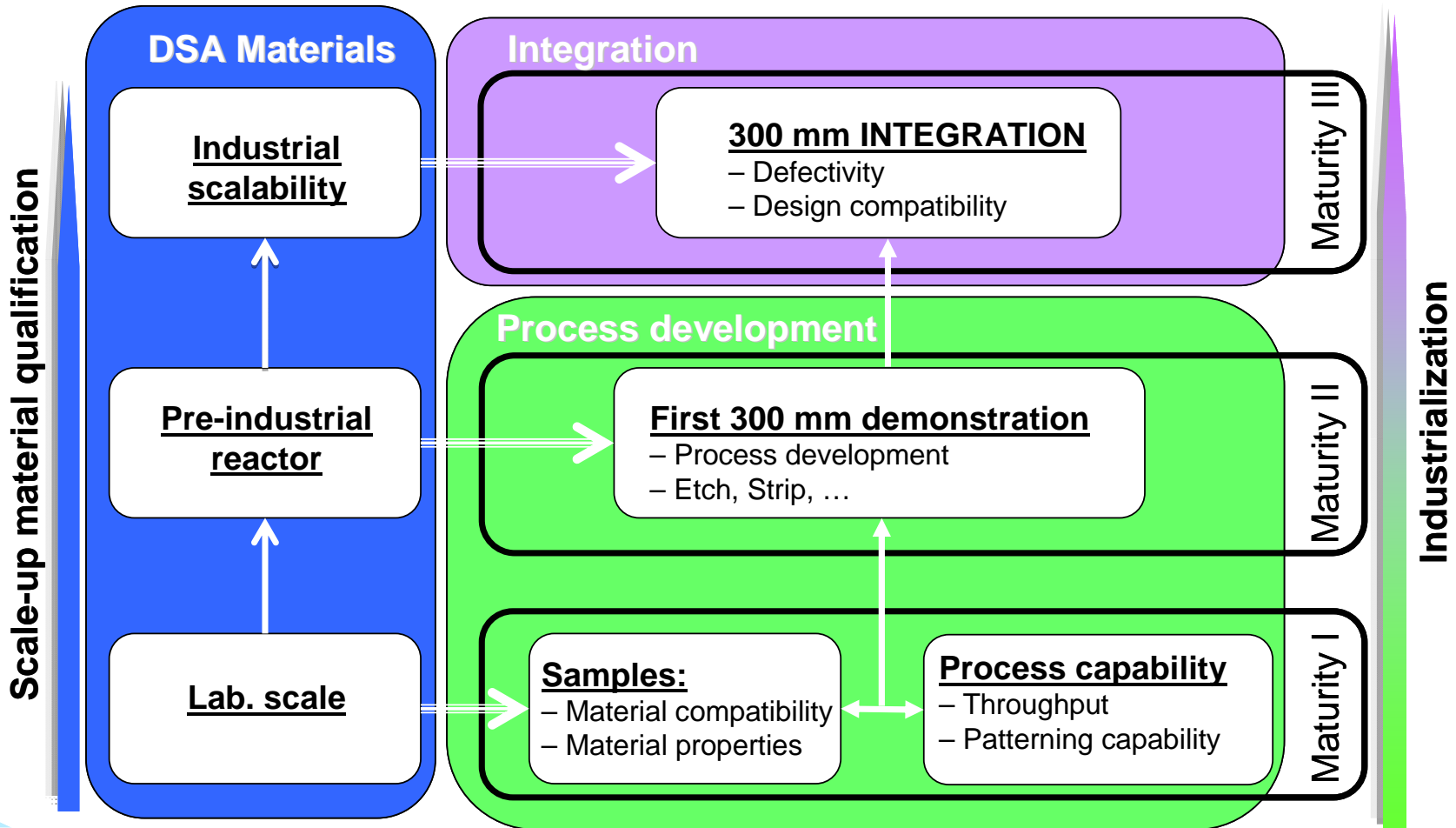
missions ?

- Push material platforms to maturity
 - From lab scale to industry
 - Evaluate advanced copolymer platform
- Develop 300mm patterning solutions
 - Certify material compatibility with clean room standard
 - Screen DSA material performances
 - Verify transfer capabilities
- Scale-up DSA processes to production level
 - Compatibility with design rules
 - Respect of ITRS standard : defectivity, throughput...



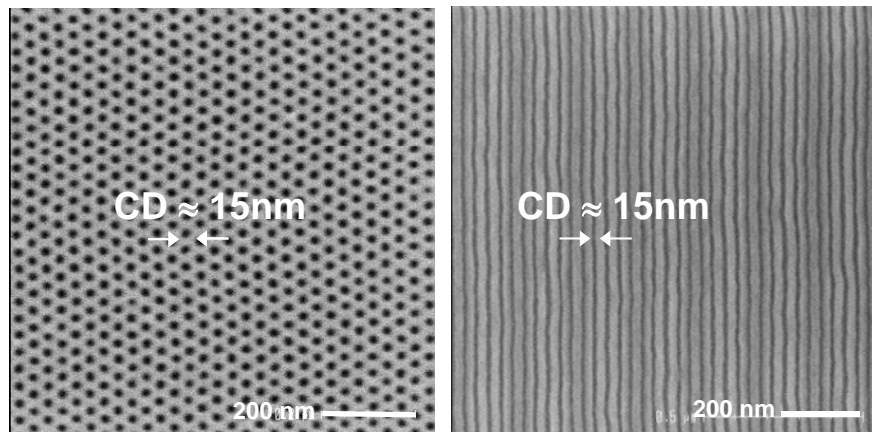
How to go from R&D to industrial ?

A production-oriented consortium

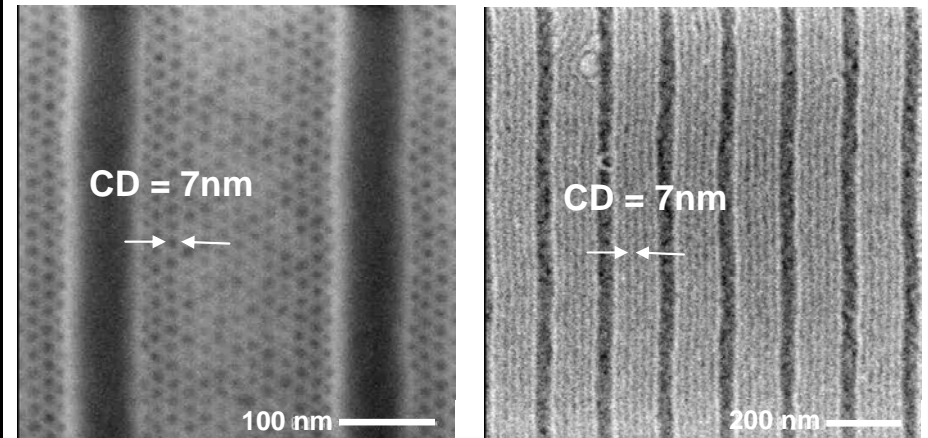


ARKEMA – LETI partnership : materials path

- Efficient neutralization layer
- Several materials under screening
 - PS-PMMA platform
 - High χ platform



PS-b-PMMA BCP



High χ BCP



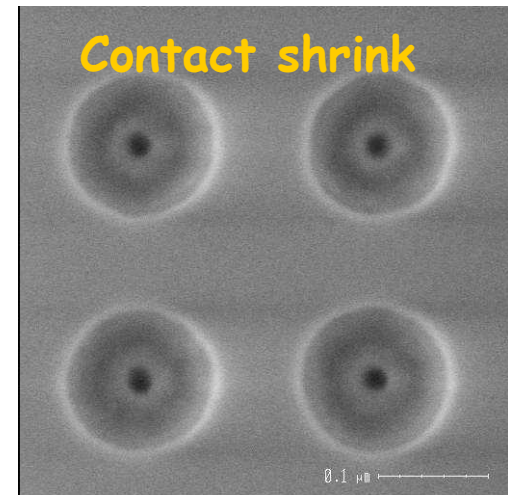
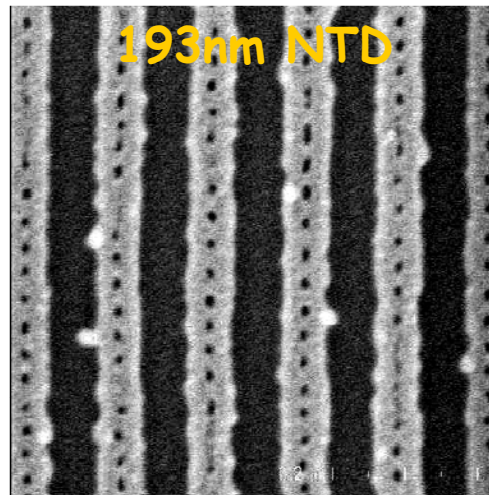
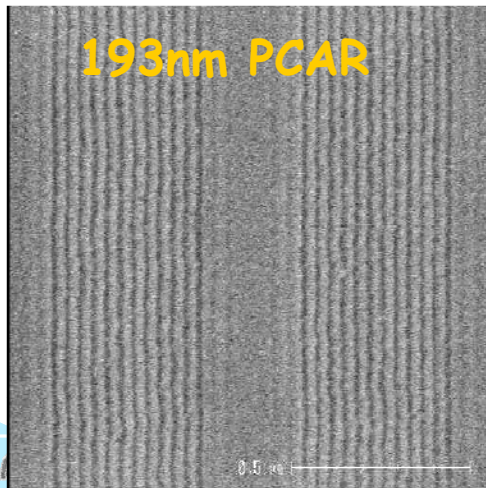
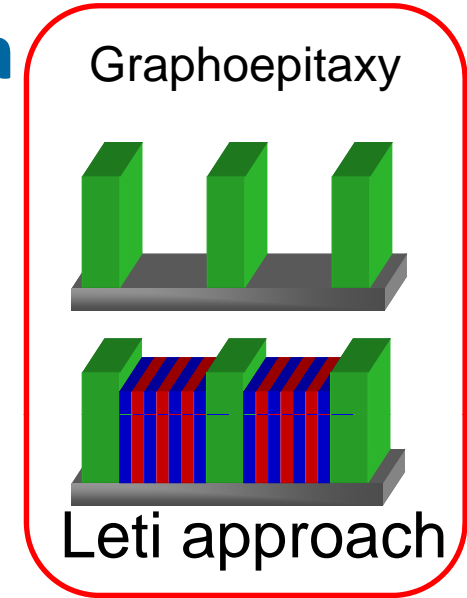
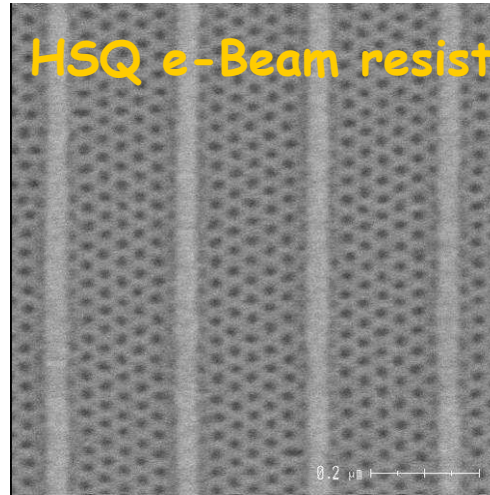
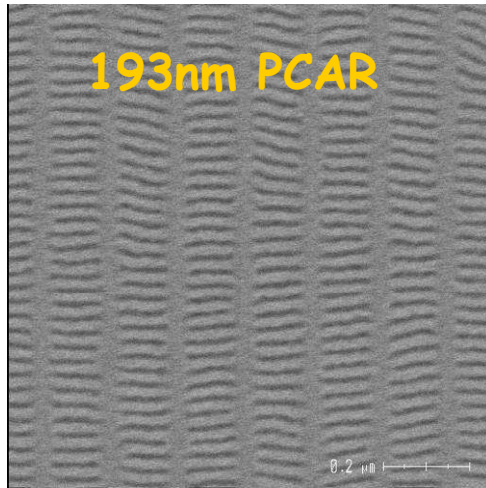
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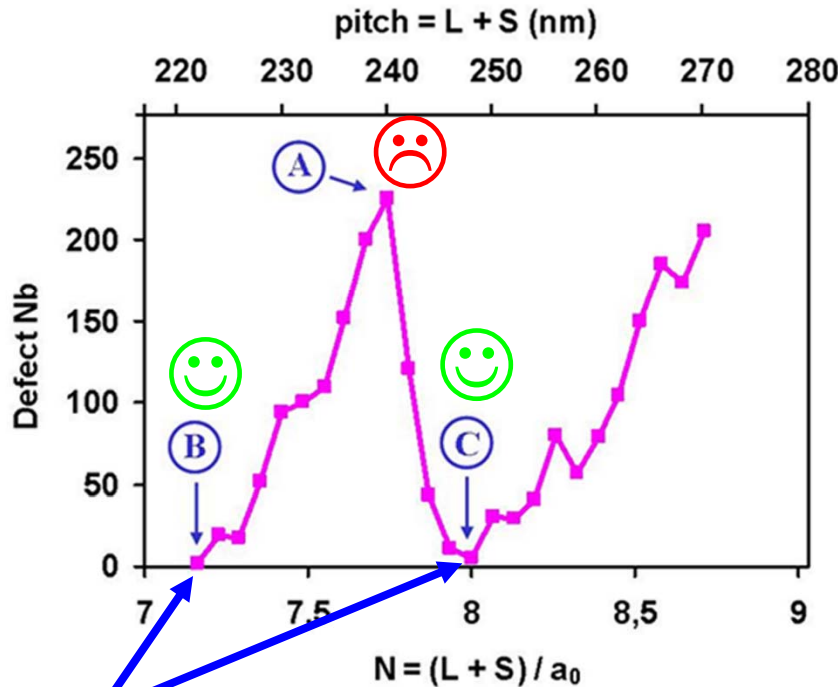
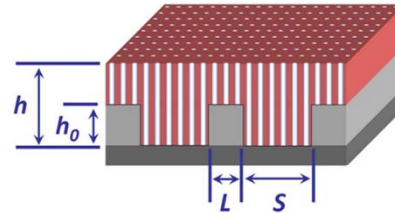
Why grapho-epitaxy preference ?

A versatile process LETI demonstration

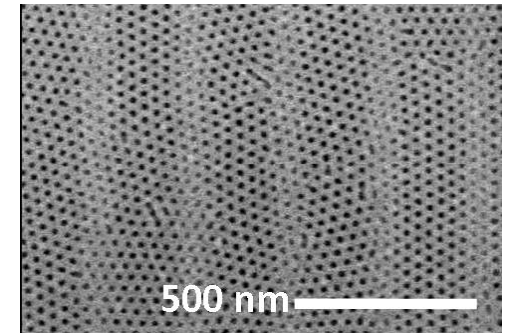


How to find optimum guiding litho process ?

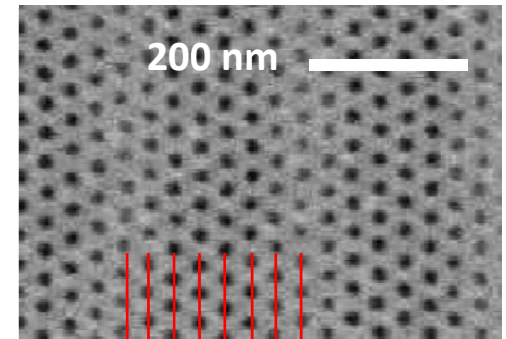
=> Influence of Litho1 design rules & BCP material



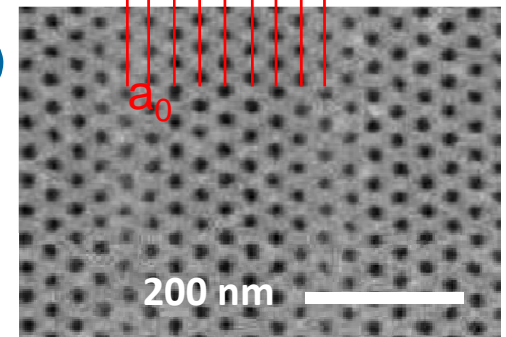
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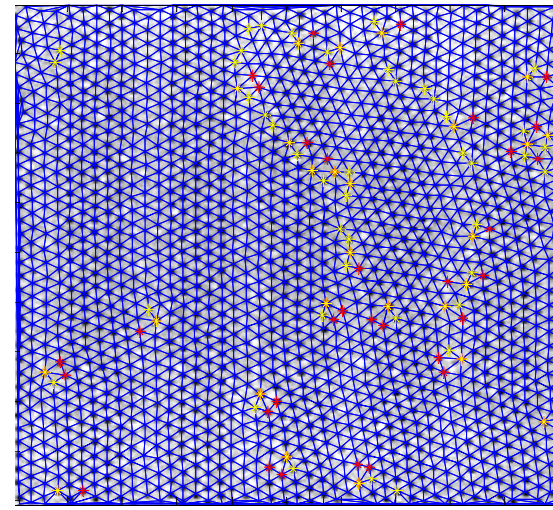
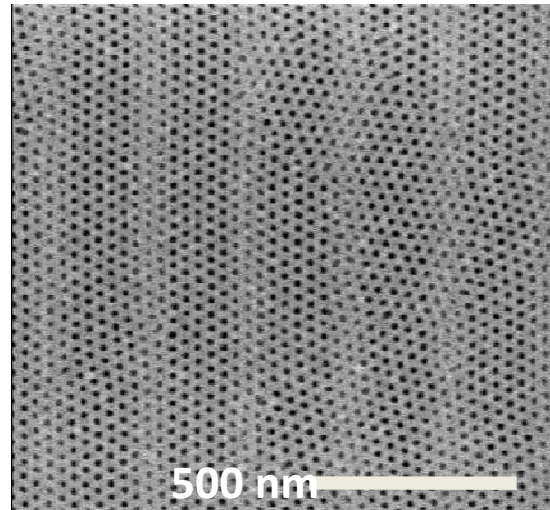


Design rule compatibility

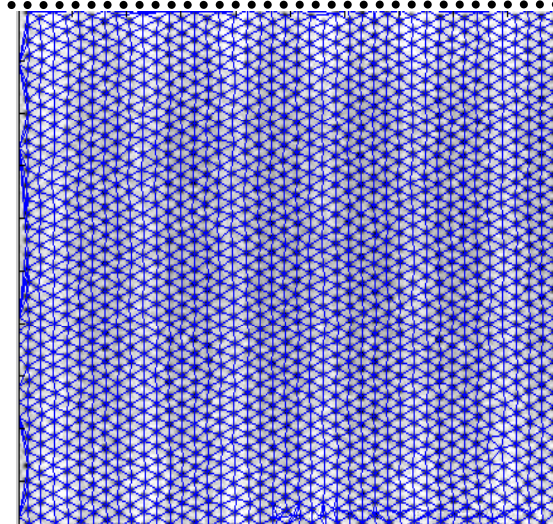
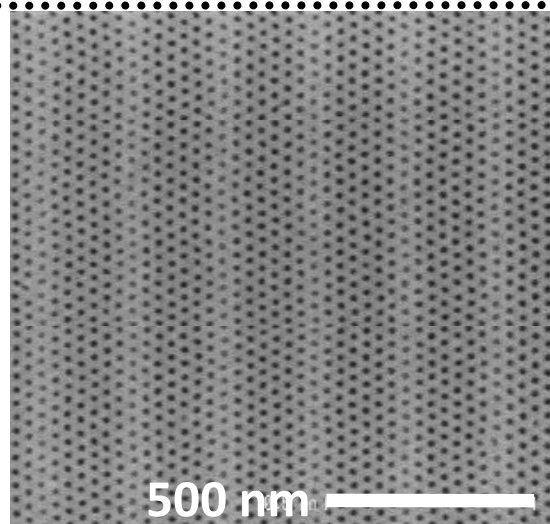
“Optimization of block copolymer self-assembly through graphoepitaxy: A defectivity study” R.Tiron et al., JVST B29 06F206 (2011)

Zero Defect Configuration

Before litho1 optimization



After litho1 optimization

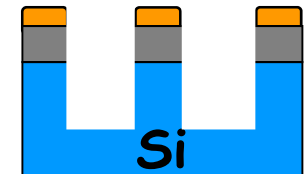
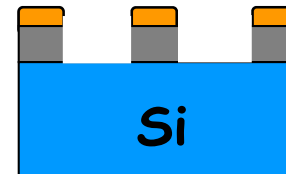
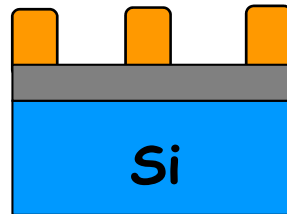
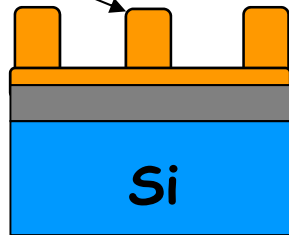


Defectivity measurement enables lithography and process optimization

Silicon Etching with Copolymer Lithography

Initial mask (PS)
30 to 100 nm thick

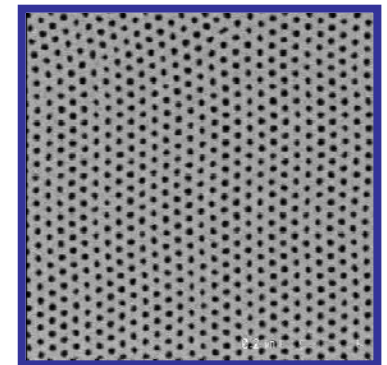
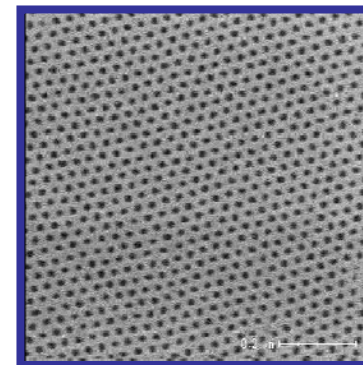
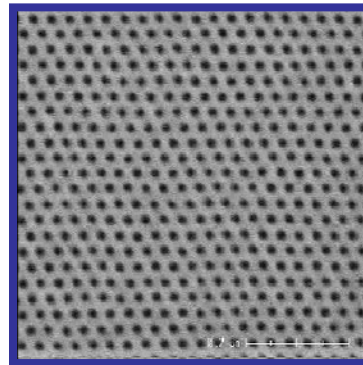
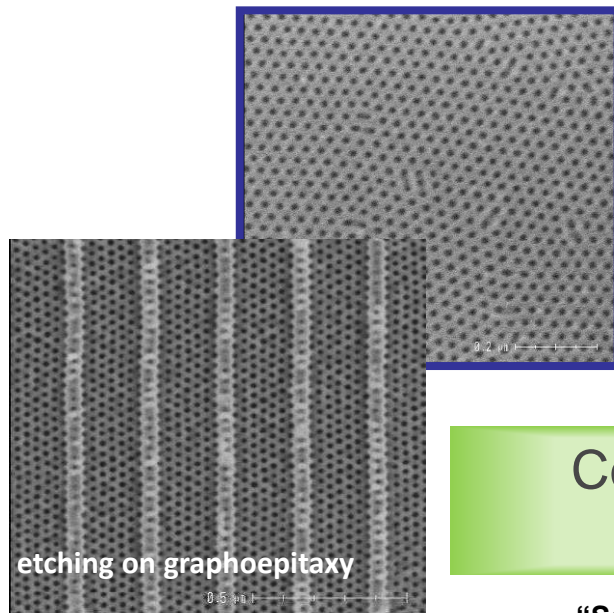
SiO₂ Mask
(10 nm)



- Brush opening (Ar/O₂ plasma)
- PS plasma treatment

- Mask etching (CF₄ based plasma)

- Silicon etching (HBr/Cl₂/O₂ plasma)



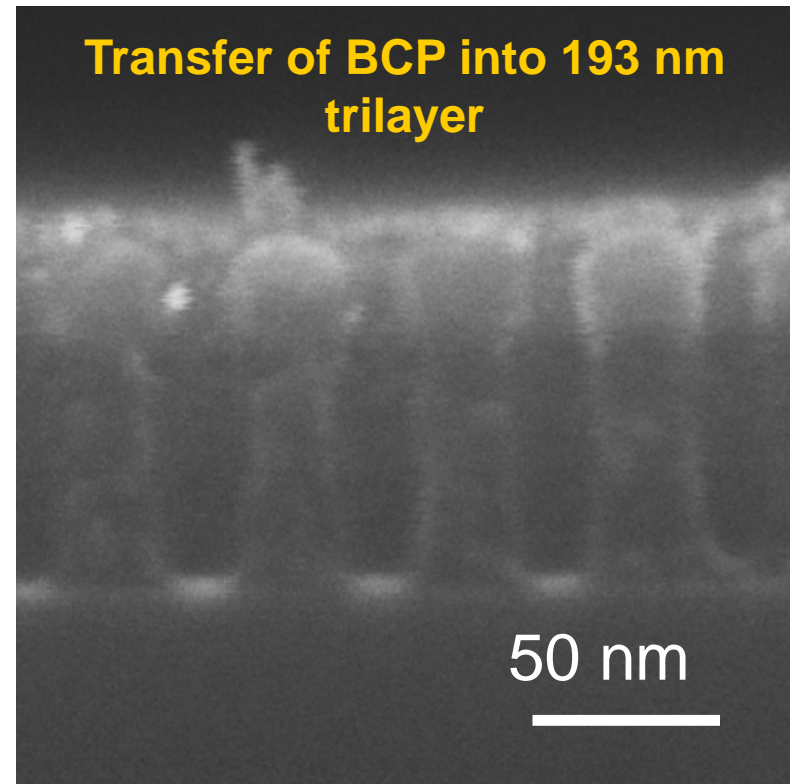
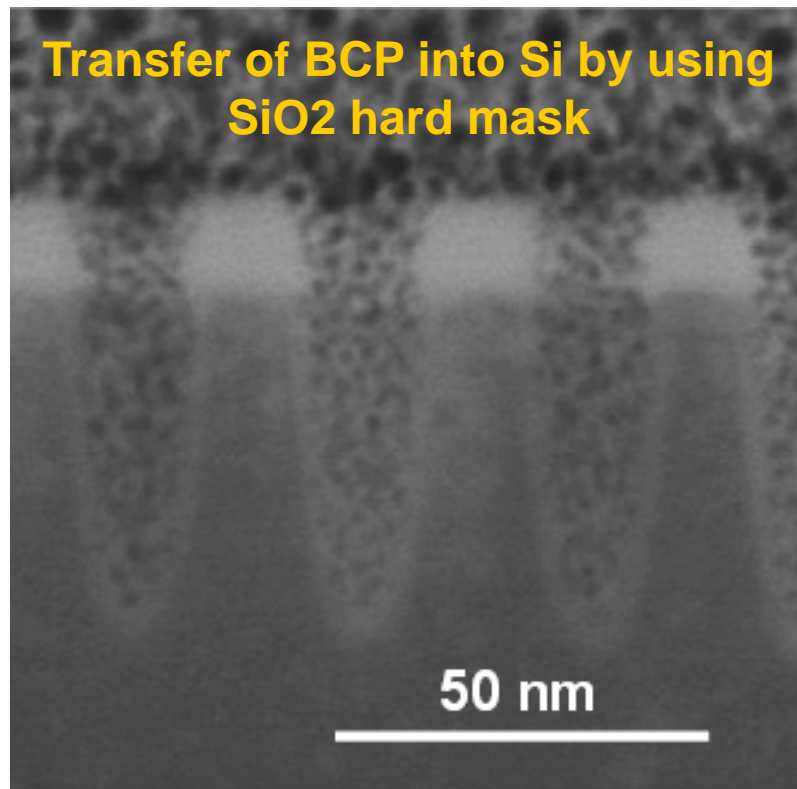
Copolymer etching process fully compatible with CMOS requirements


“Self-assembly patterning using block copolymer for advanced CMOS technology: optimisation of plasma etching process”

Thierry Chevolleau, CNRS (France)- Paper 8328-20, SPIE2012



Silicon Etching with Copolymer Lithography



 Copolymer etching process fully compatible with CMOS requirements

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Contact shrink and multiplication using DSA of BCP

After 193nm litho.



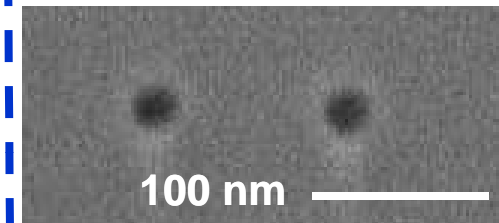
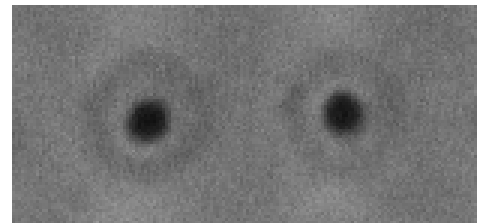
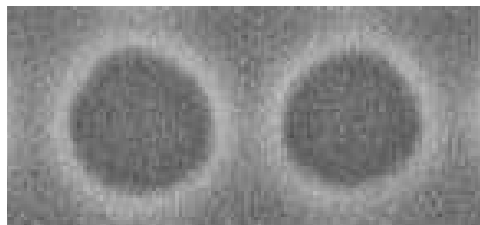
After BCP DSA



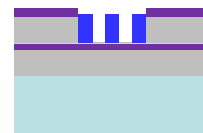
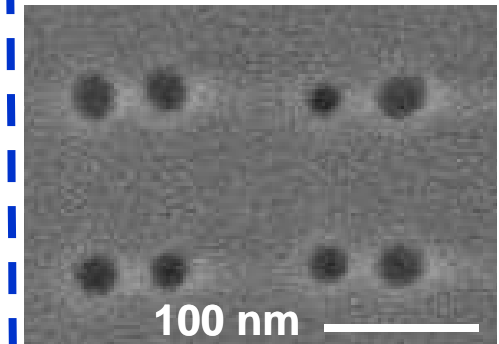
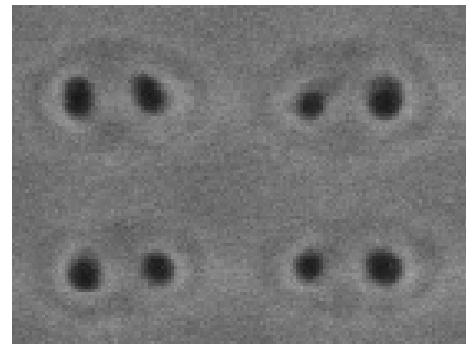
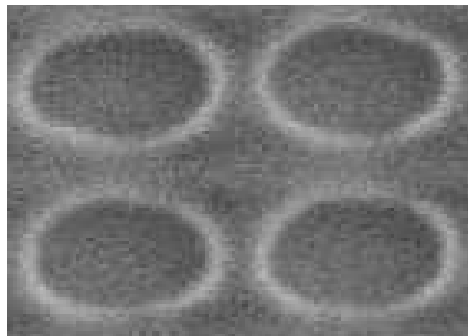
After BCP etching



Contact Shrink

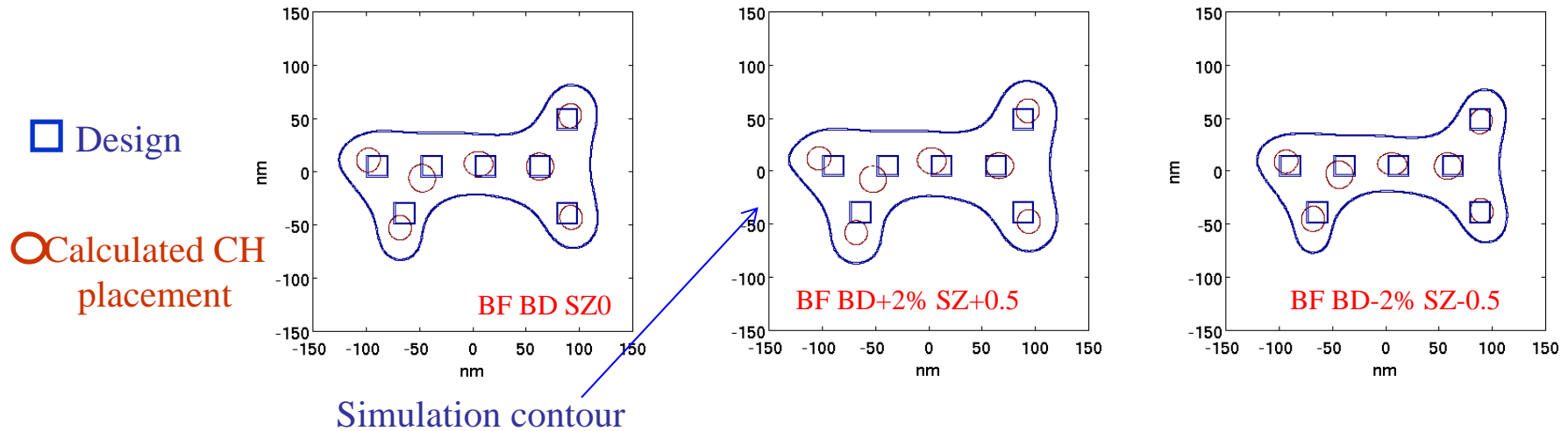


Contact Multiplication



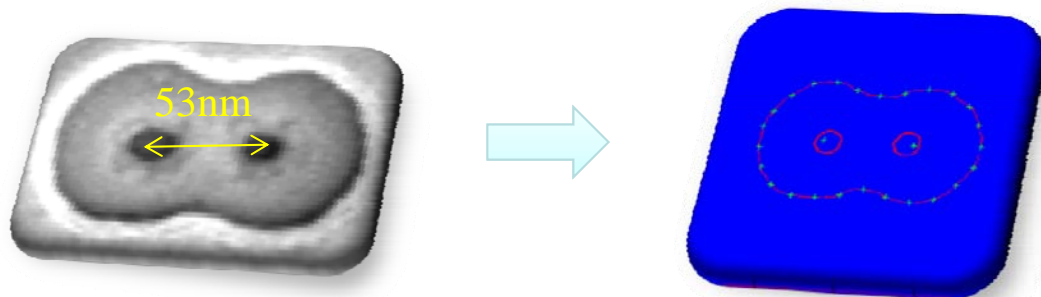
Integration (litho+etch) demonstrated for contact shrink and multiplication

How to define design rules: Example of code



Contour variation w.r.t. dose, focus and mask CD error variations

Experimental validation



- + - Extracted Contour
- + Calculated CH position
- CH position on wafer



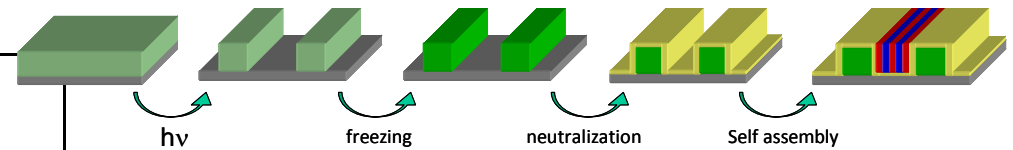
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DSA 300 mm infrastructure on SOKUDO RF³ track

| Process steps | CMOS requirements |
|----------------------|---|
| Guided litho | ➤ Resist hardness to bake and solvent |
| PS-r-PMMA spin coat. | ➤ metal/ ionic contamination ➤ solvent compatibility |
| Grafting | ➤ Bake time and temp. |
| Rinse | ➤ solvent compatibility |
| Copolymer coating | ➤ metal/ ionic contamination ➤ solvent compatibility |
| Self assembly | ➤ Throughput ➤ Defectivity |
| Etching | ➤ Transfer capabilities |



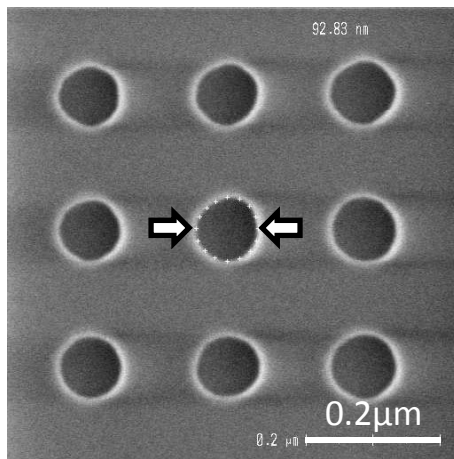
Front-end production
300mm track & scanner

“Pattern density multiplication by direct self-assembly of block copolymers: toward 300mm CMOS requirements” Raluca Tiron et al, CEA-Leti (France) - Paper 8324-23, SPIE2012

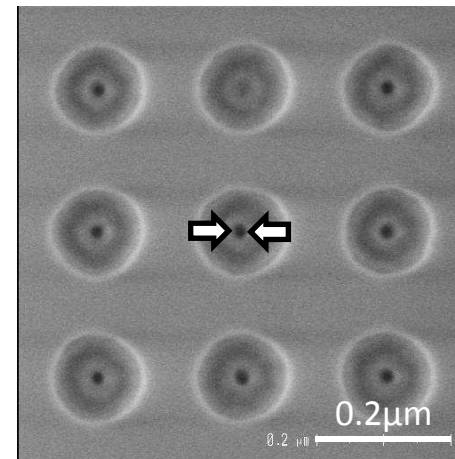


Shrink of contact holes 300mm process

graphoepitaxy with standard lithography 193nm



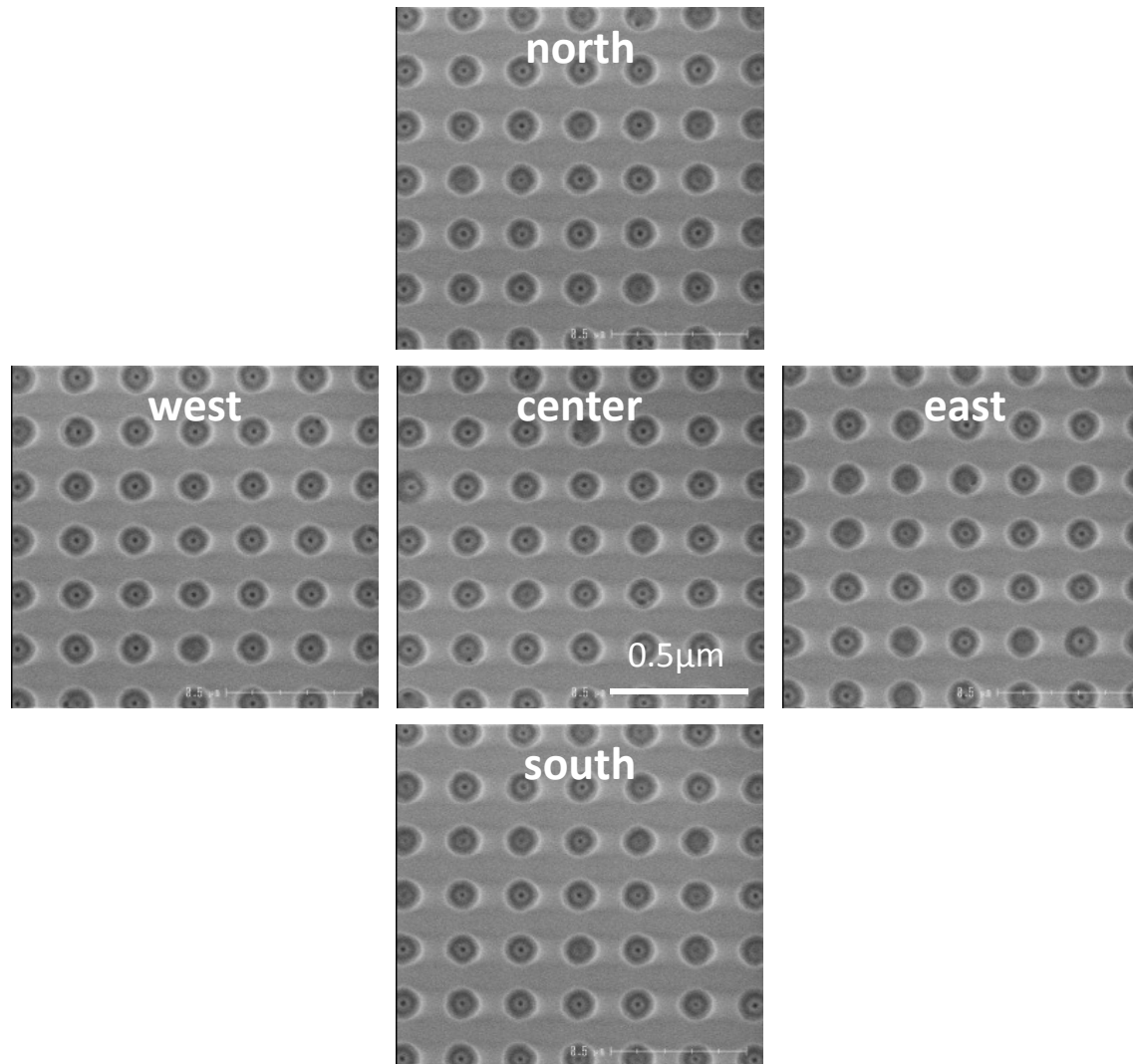
CD ~ 100nm



CD ~ 15nm



Shrink of contact holes 300mm process



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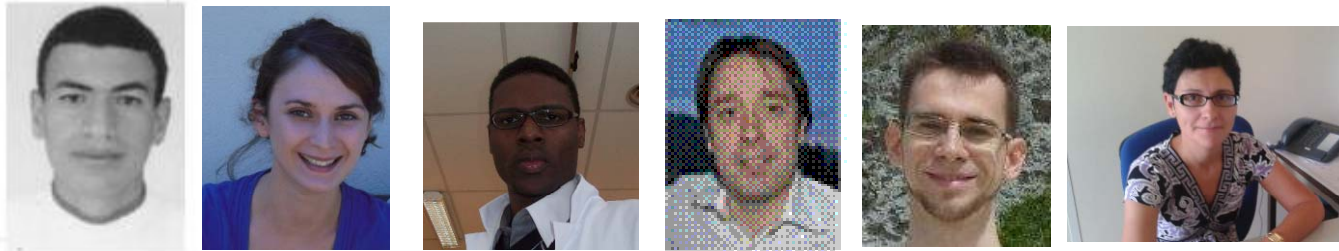
To conclude

- DSA a complementary lithography technique that could get inserted as early as the 14nm node
 - In a first step by using PS-b-PMMA like materials
 - In a second step by using high χ materials
- A realistic application: contact hole shrink and doubling
- Defectivity is key

Thanks for SOKUDO involvement and support



All this is possible thanks to:



A.Gharbi, P.Pimenta-Baross, J. Dubray,
S.Barnola, J.Belledent, S.Moulis, R.Tiron *LETI*
X.Chevalier, M.Argoud, C.Navarro *Arkema*
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G.Fleury, G.Hadziioannou, LCPO



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