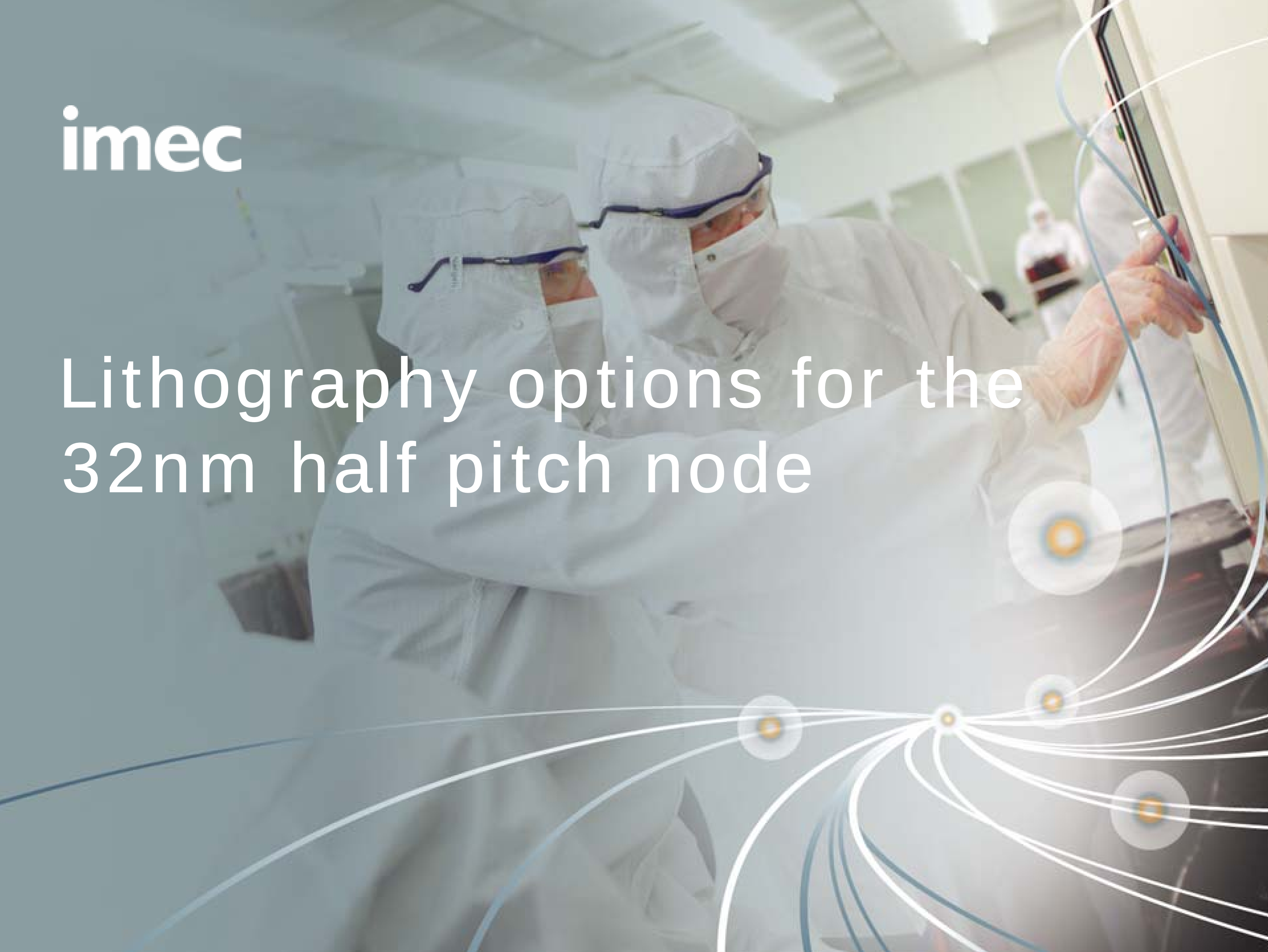


imec

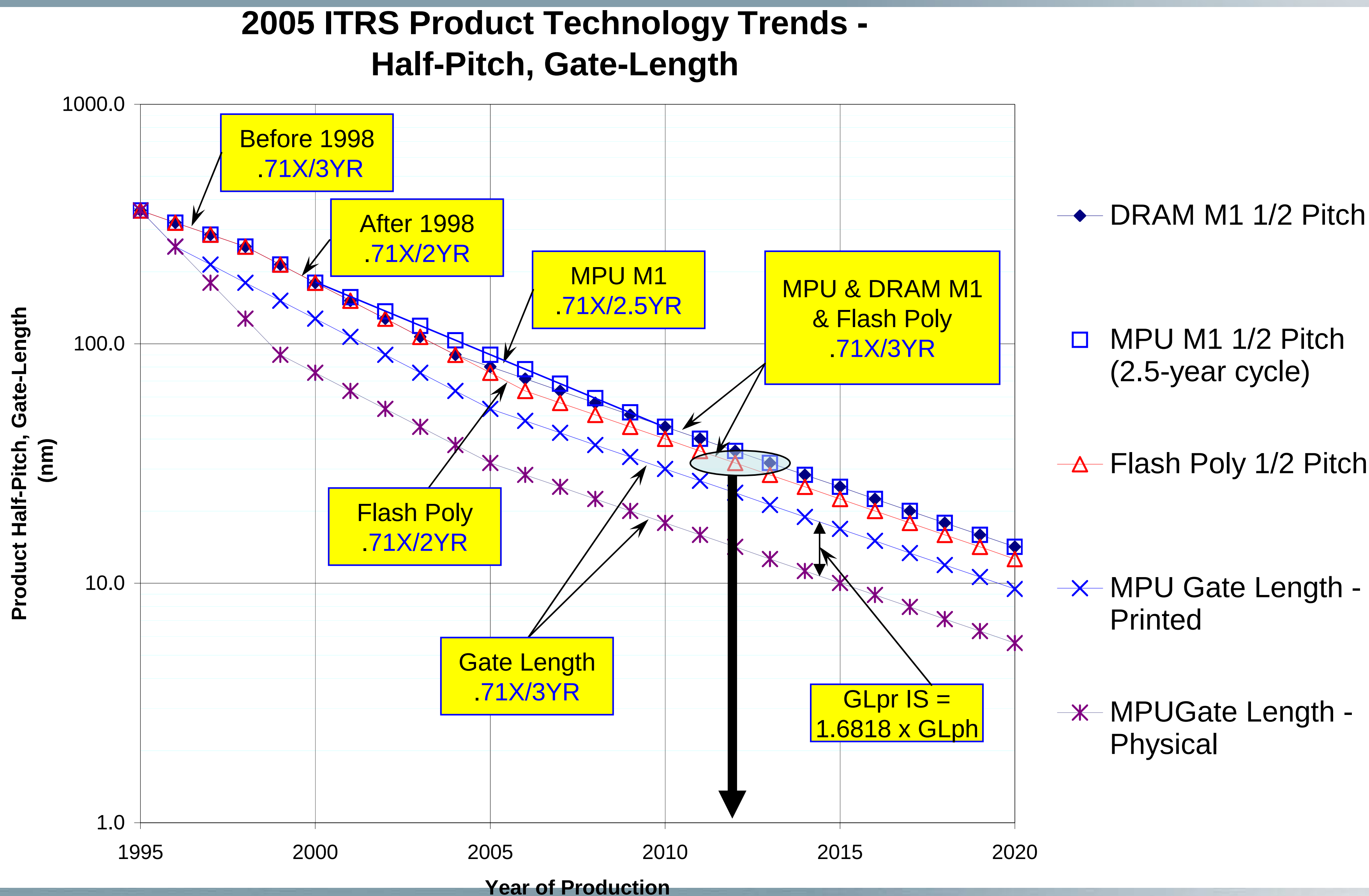
Lithography options for the 32nm half pitch node

imec

Lithography options for the 32nm half pitch node

Luc Van den hove and Kurt Ronse

ITRS roadmap:32 nm half pitch requirement



32nm half pitch options

$$resolution = k_1 . \frac{\lambda}{NA}$$

NA	k_1	λ
ArF Immersion 1.65 NA (k_1=0.275) Single exposure	ArF Immersion with double patterning 1.35 – 1.40 NA (k_1=0.20)	EUVL 0.25 NA (k_1=0.6) Single exposure

Technical challenges:

Lens complexity *New liquid (n_f>1.8)* *New optical material (n>1.9)*	Overlay requirement Process integration	Source power Optics lifetime *Resist infrastructure* *Mask infrastructure*

Outline

- Introduction
- 193 nm immersion lithography
- EUV Lithography
- Double patterning
- Conclusions

193nm immersion lithography

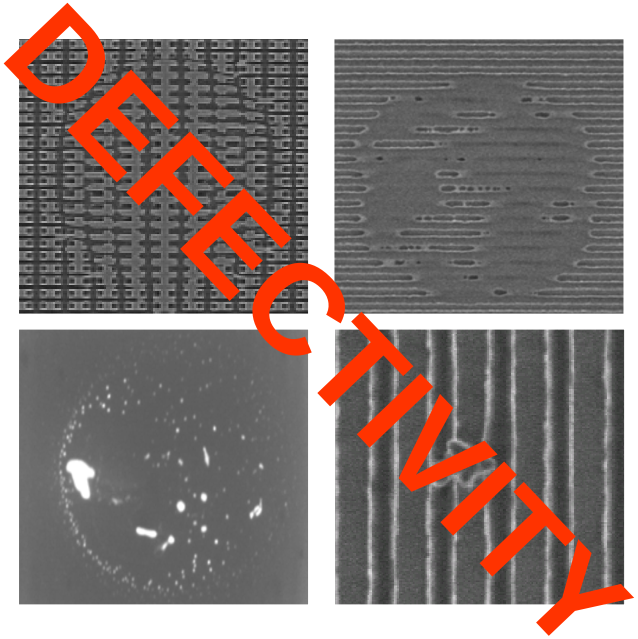
from RESEARCH IDEA… **to DEVELOPMENT**

in WORLD RECORD TIME

193nm immersion lithography

from DEVELOPMENT…

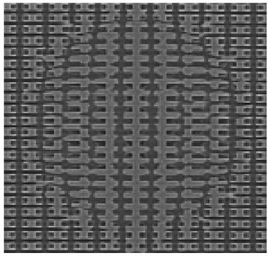
to MANUFACTURING ???



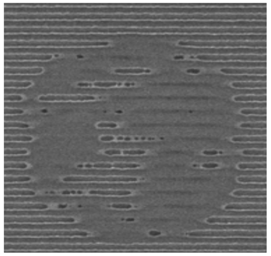
Is immersion ready ?

Status 193nm immersion lithography

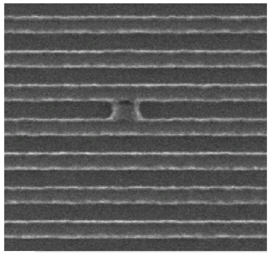
Defectivity



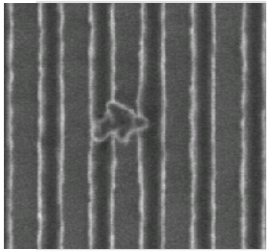
Air bubbles



Water marks and drying stains



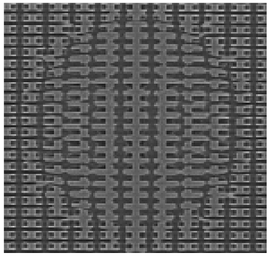
Resist / TC – water interaction



Particles

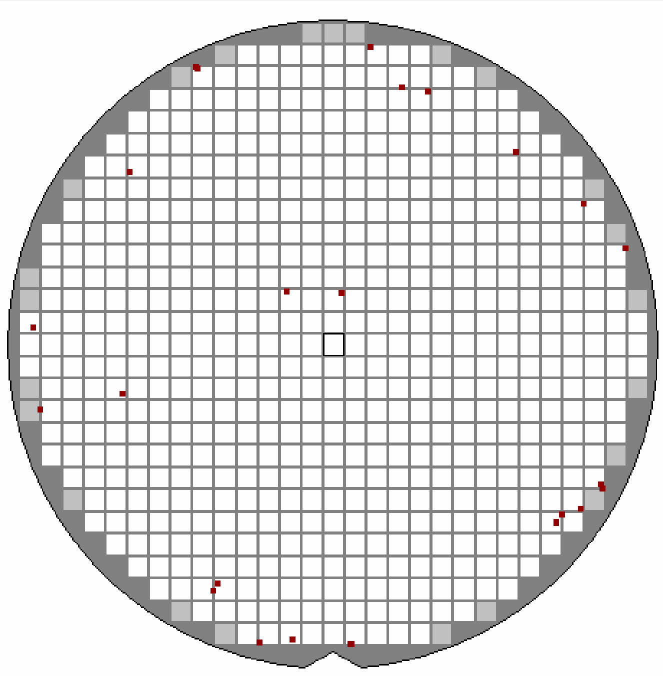
Status 193nm immersion lithography

Defectivity



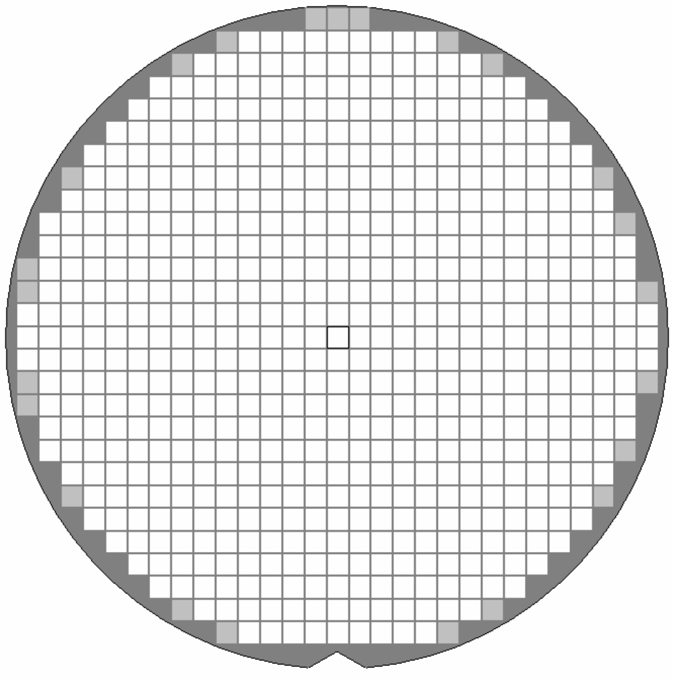
Air bubbles: no longer an issue

Early config.



24 bubbles

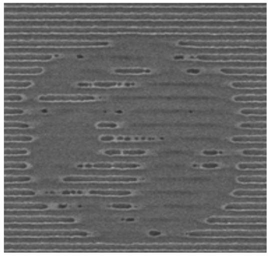
Latest XT:1250i config.



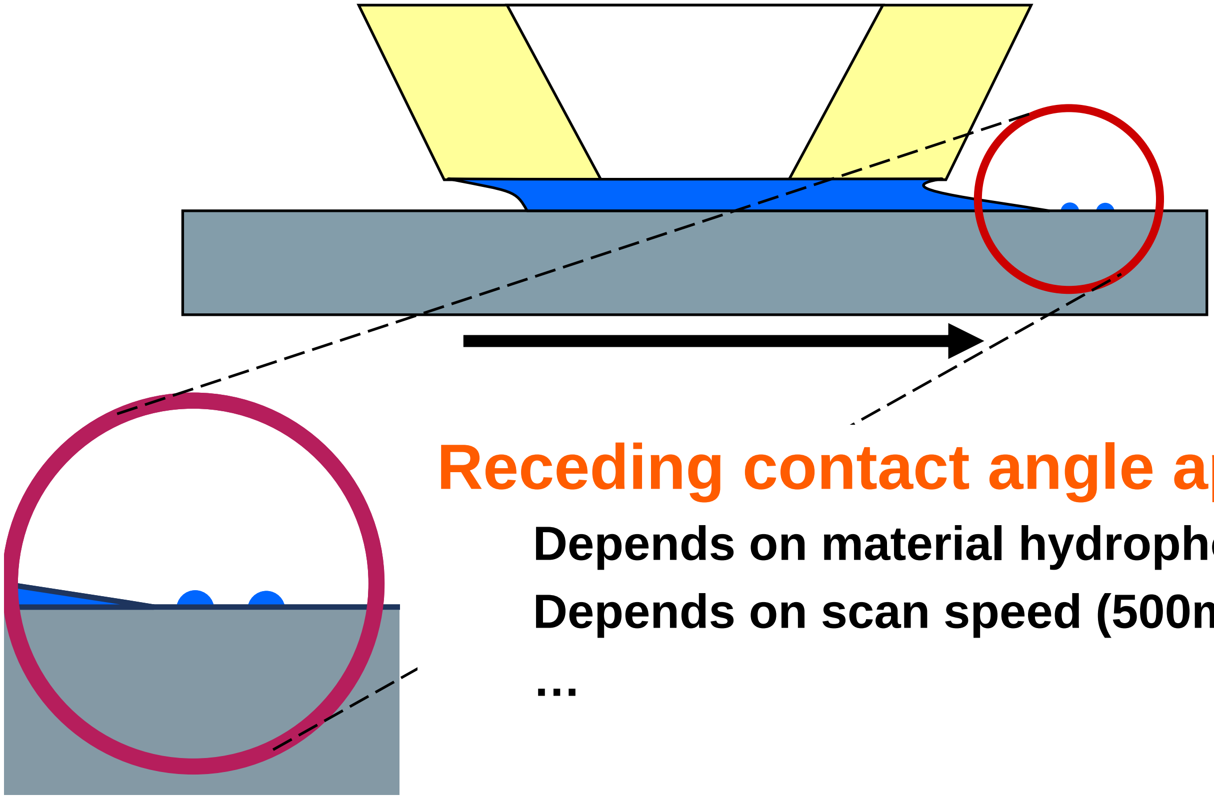
0 bubbles

Status 193nm immersion lithography

Defectivity

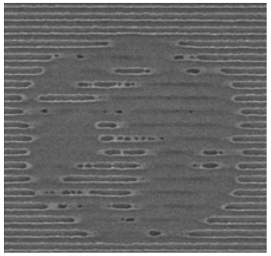


Water marks and drying stains

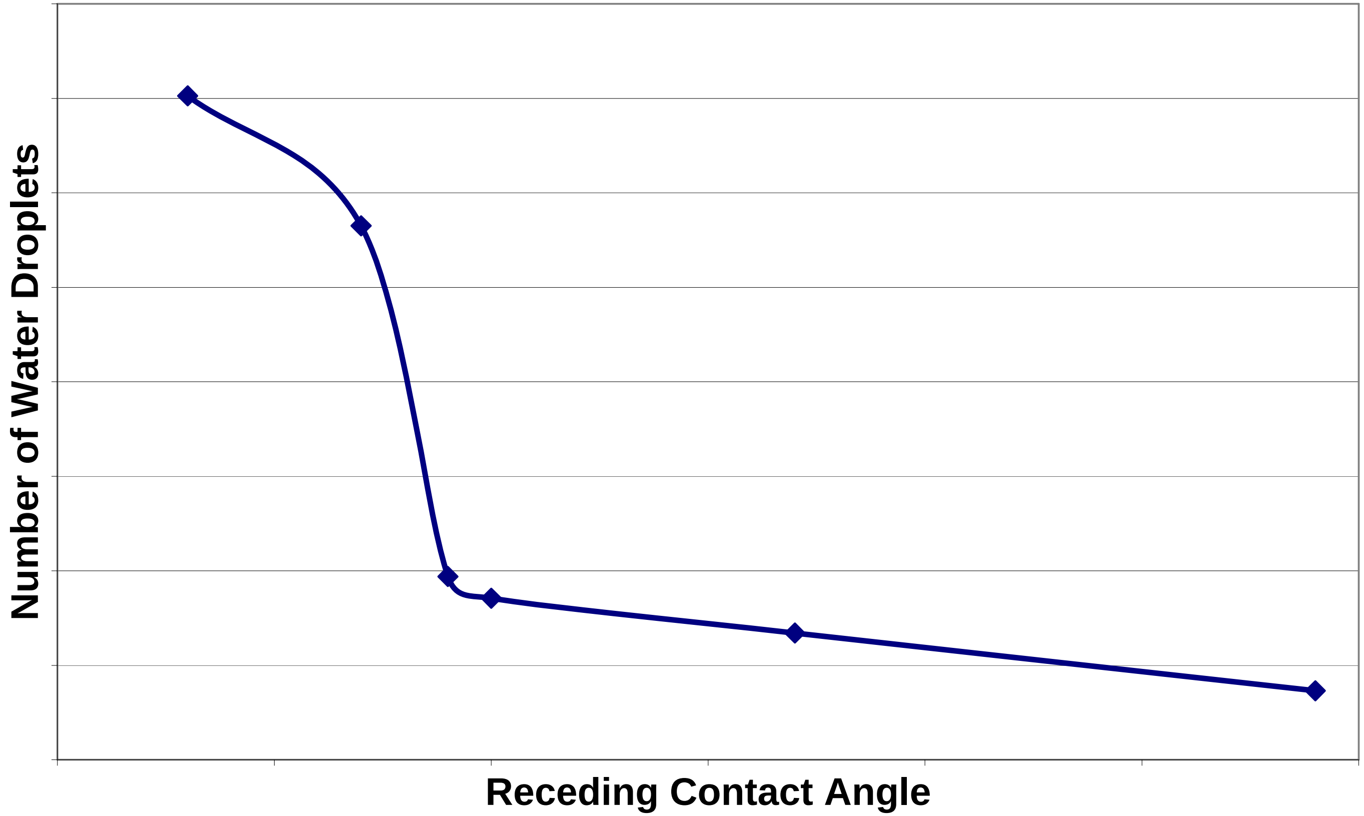


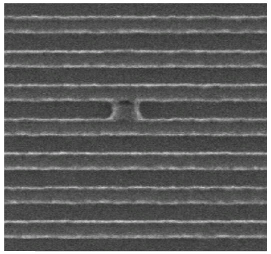
Receding contact angle approaching 0

- Depends on material hydrophobicity
- Depends on scan speed (500mm/s)
- …



Water marks and drying stains





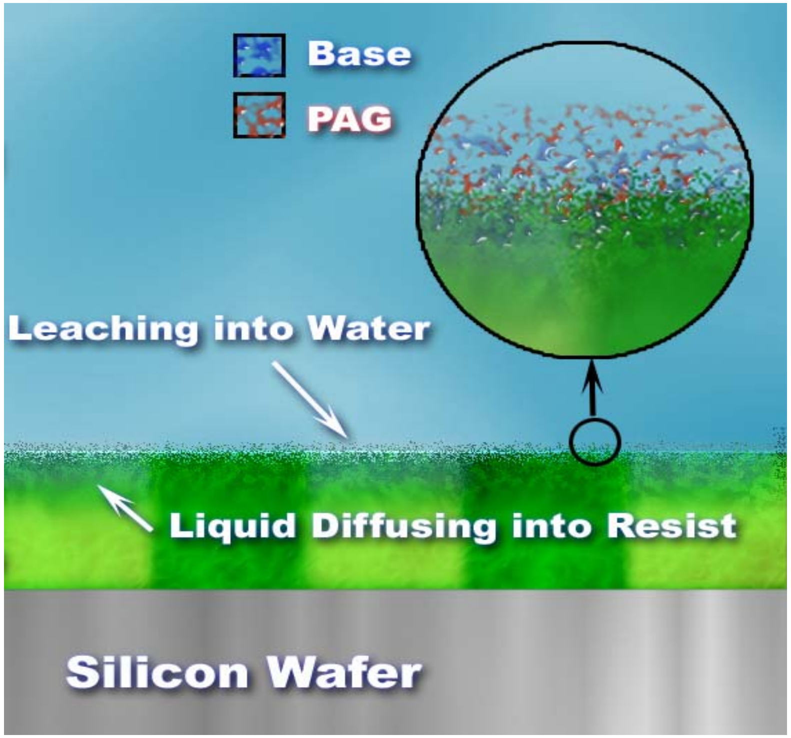
Resist / TC – water interaction

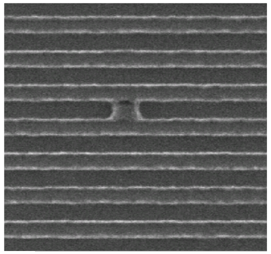
Leaching

of resist components in the water

Water uptake

by resist / TC…

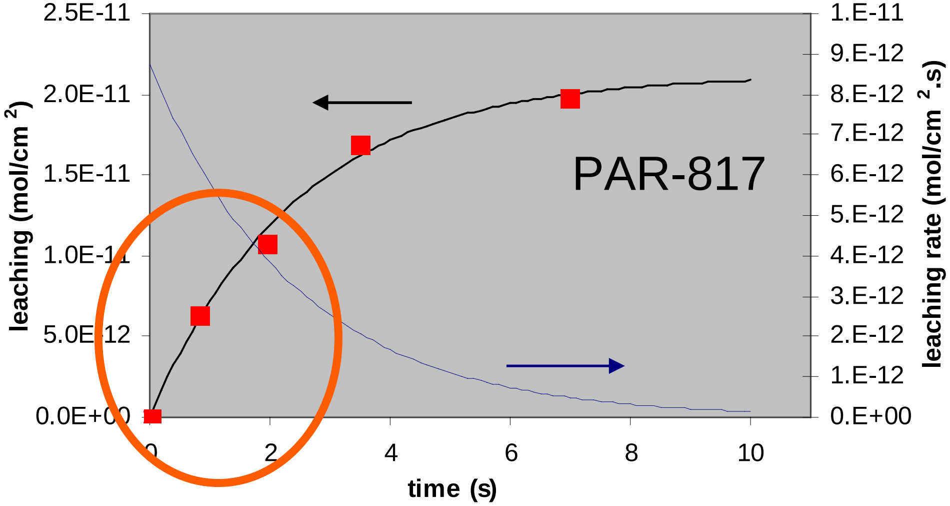




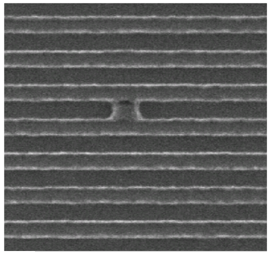
Resist / TC – water interaction

Leaching status

Method in place for dynamic leaching measurements



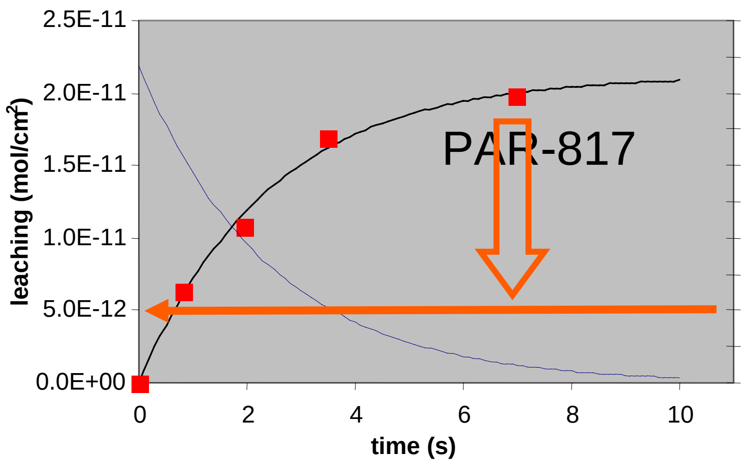
Amount of leaching during first 1-2 seconds is key
(for a high throughput immersion scanner)

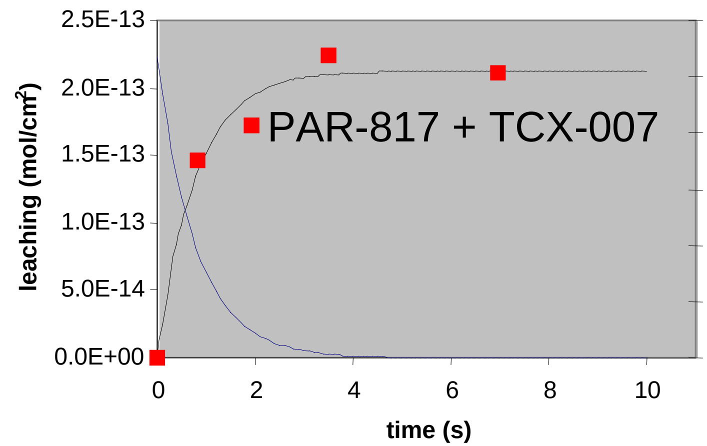


Resist / TC – water interaction

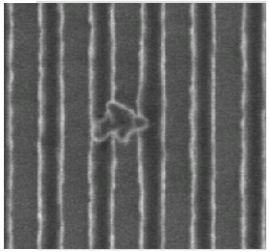
Leaching status

- Method in place for dynamic leaching measurements
- Top coats very efficient in preventing leaching (~100 x less)





- Leaching currently prime reason to use top coat
- Recent immersion specific resists much lower leaching (factor 4) (5.10^{-12}mol/cm plateau)



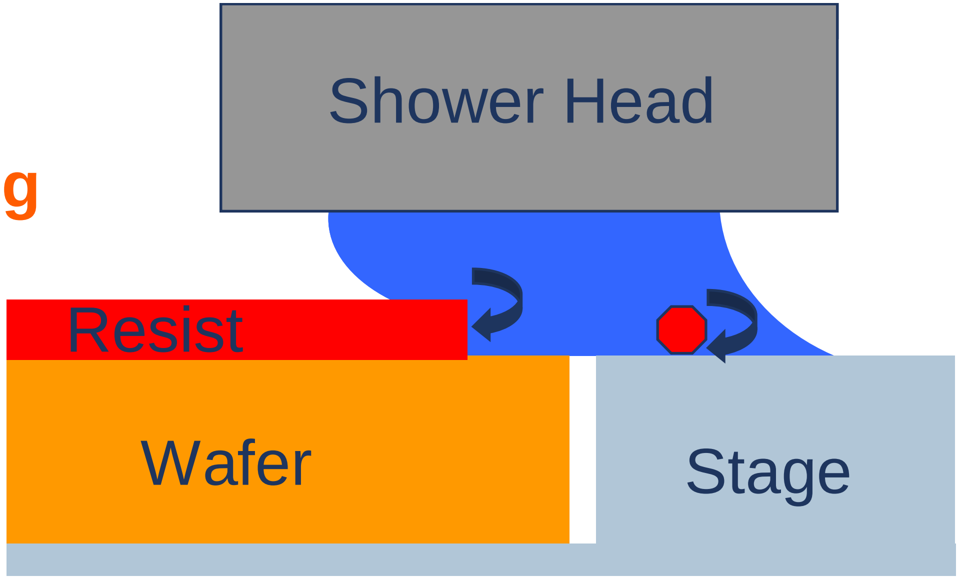
Particles

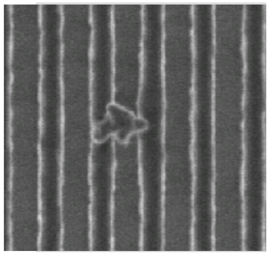
Wafer edge film peeling

Edge bead engineering !

Particle transport

from chuck onto wafer



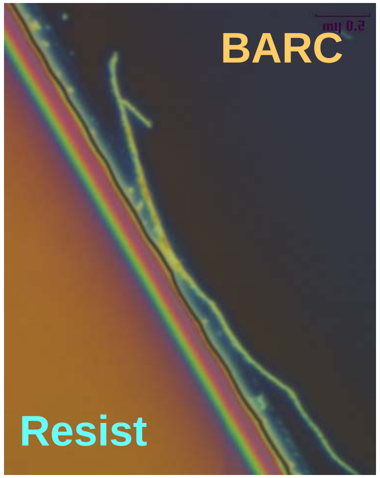


Particles

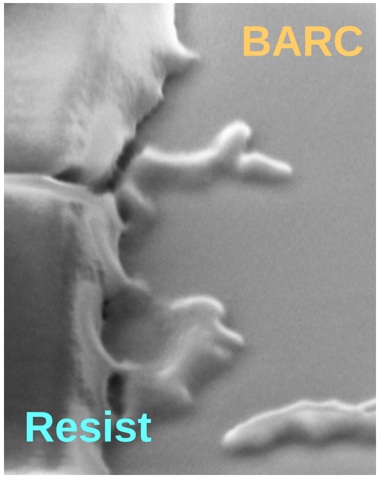
Wafer edge film peeling

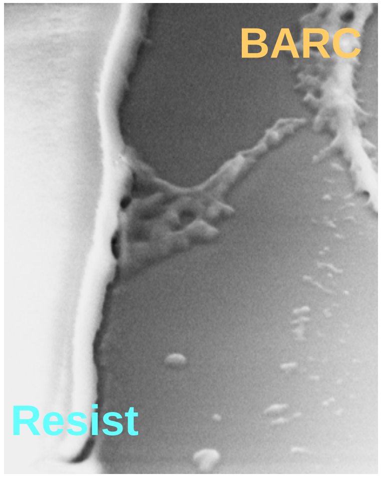
Edge bead engineering !

Before exposure



After exposure
Before develop

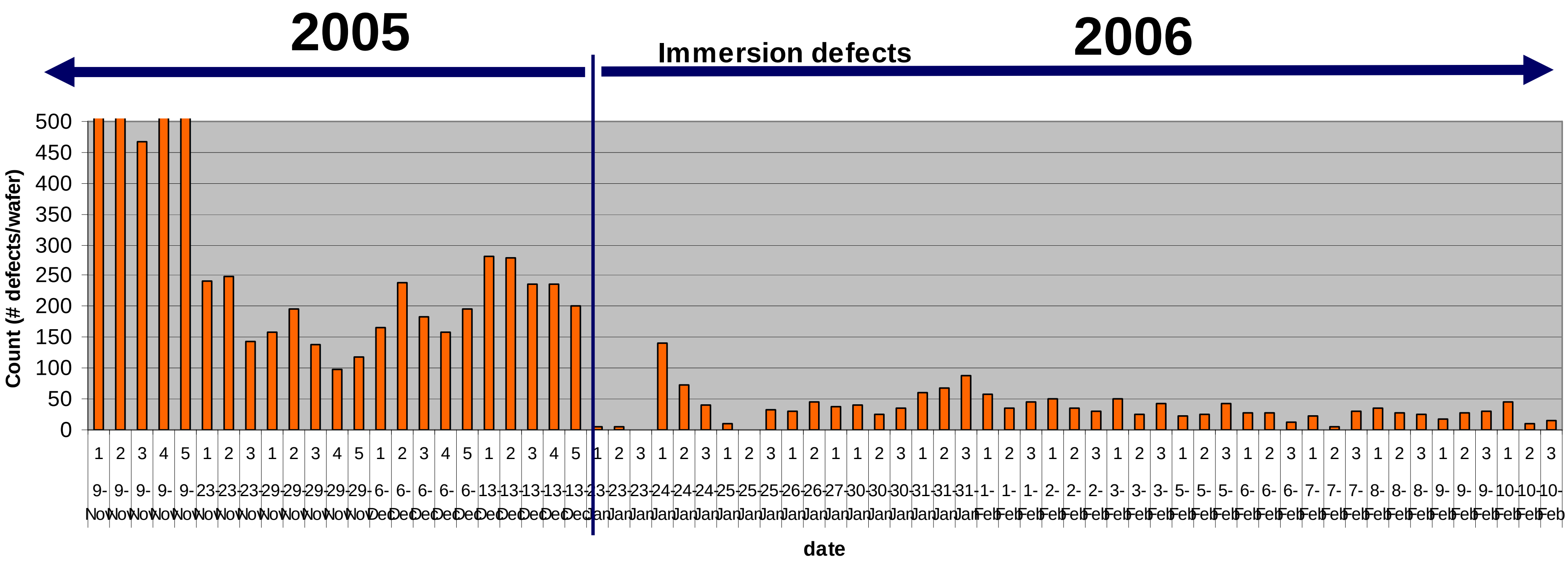




SEM after develop

Breakthroughs by strong partnership

Defect reduction trend (daily monitor)

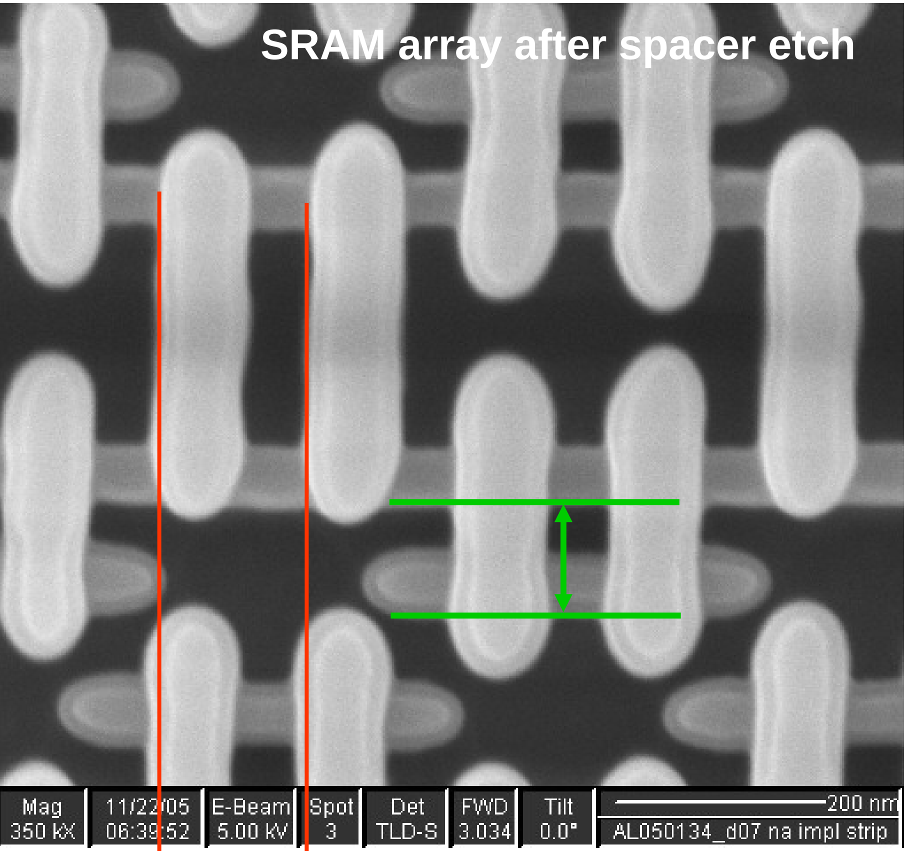


Spectacular progress over the past 12 months

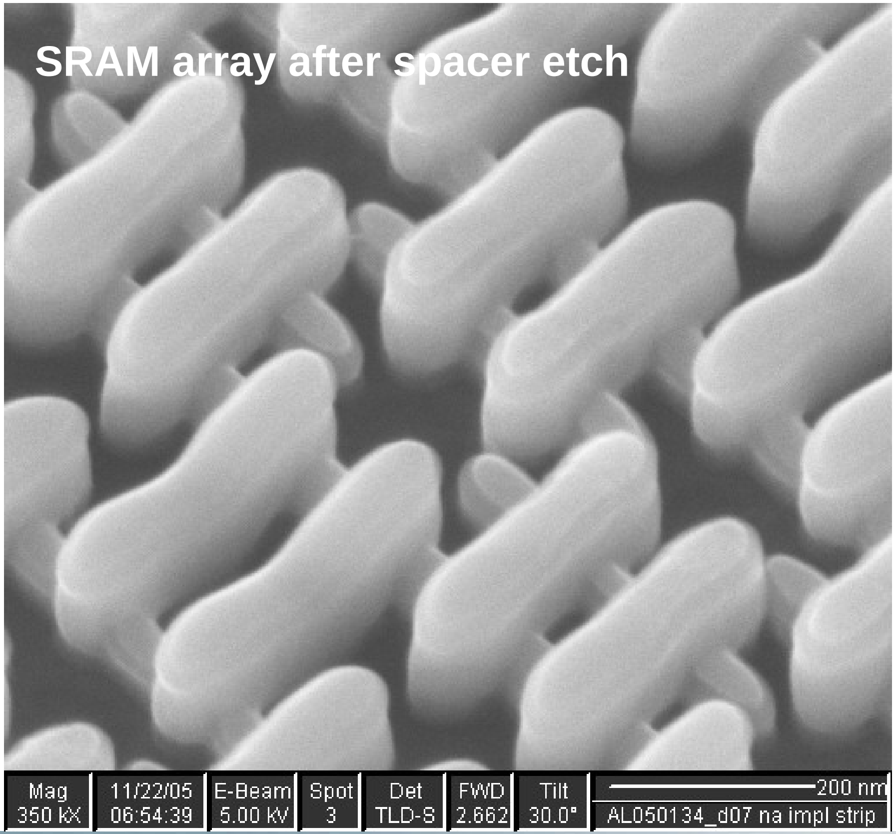
"Litho friendly 6T SRAM design"

ASML XT:1250i
0.85 NA

0.186μm^2 cell size
32nm node

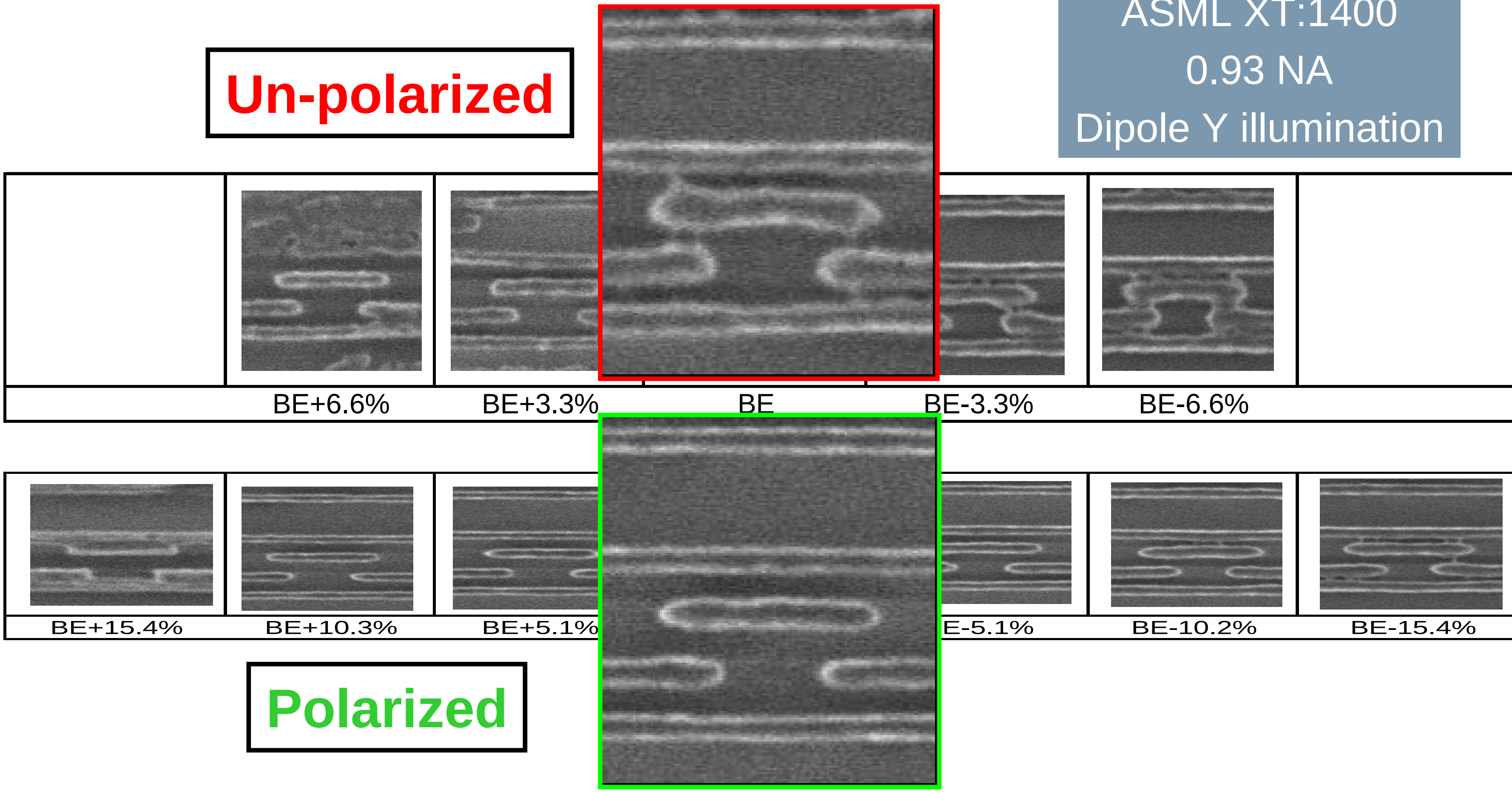


Fin hp : 62nm (0.273 k_1)
Poly hp : 75nm (0.330 k_1)



"Litho friendly 6T SRAM design"

ASML XT:1400
0.93 NA
Dipole Y illumination



Fin hp 55nm (0.265 k_1)

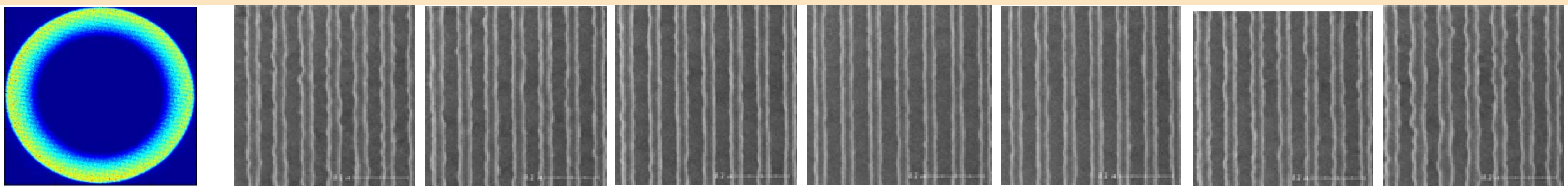
22nm node

193nm immersion lithography

Hyper NA 193i

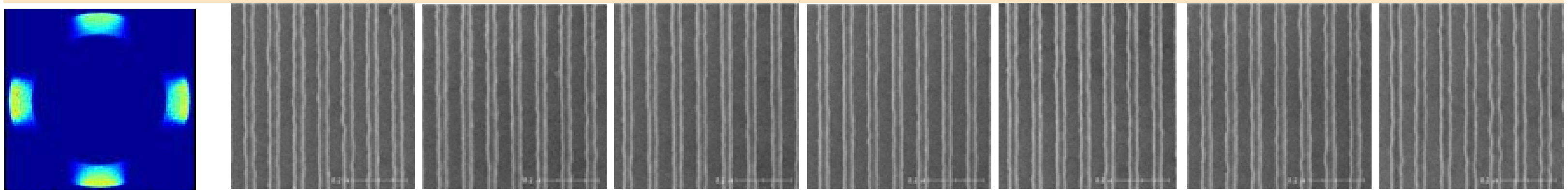
ASML XT1700i – NA=1.2

50nm **k_1=0.31** 1.2NA, σ=0.74/0.94, annular



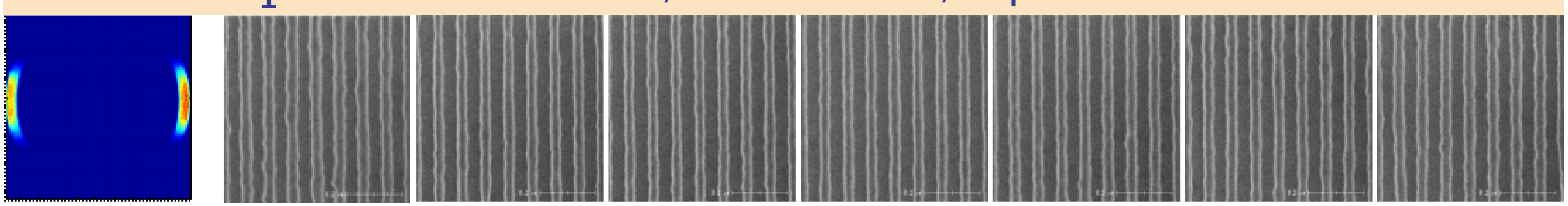
400nm DoF -210nm -150nm -90nm NF +90nm +150nm +210nm

45nm **k_1=0.28** 1.2NA, σ=0.82/0.97, C-Quad-30



500nm DoF -300nm -240nm -120nm NF +60nm +120nm +210nm

42nm **k_1=0.26** 1.2NA, σ=0.89/0.98, Dipole X-35



950nm DoF -500nm -300nm -180nm NF +180nm +300nm +450nm

193nm immersion lithography

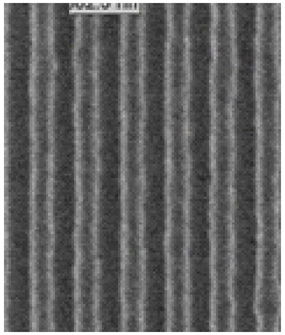
Hyper NA 193i

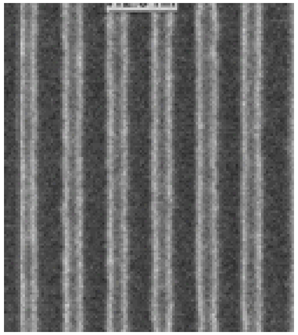
41nm, approaching 0.25k_1

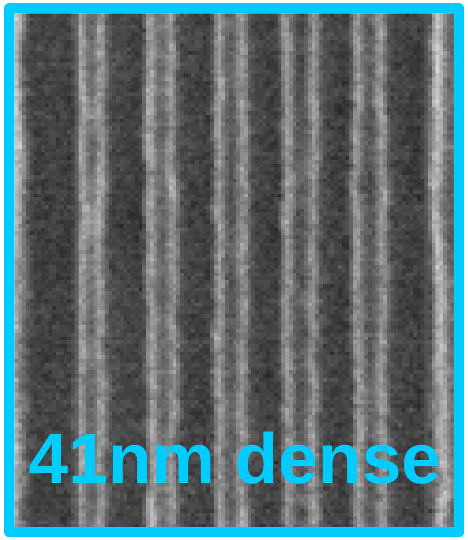
ASML XT:1700i
1.2 NA

imec

P86 – k_1 0.267 43nm dense	P84 – k_1 0.261 42nm dense	P82 – k_1 0.254 41nm dense



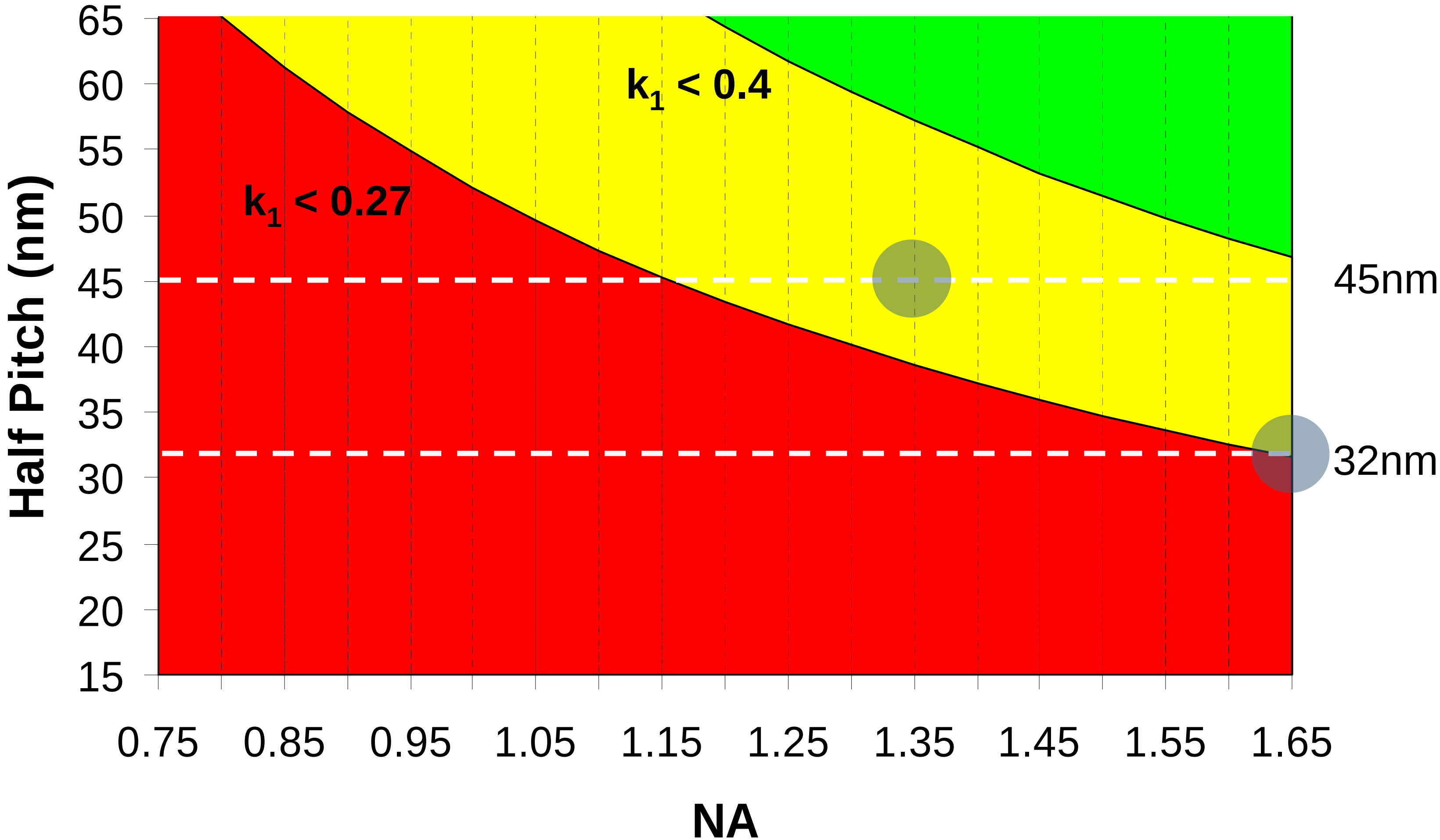




1.2NA, Y-pol, dipole X 35° s=0.98-0.89
CPL – chromeless lines
42nm barc, 120nm resist, topcoat

193nm immersion lithography
Ultimate limits

- k_1 as function of **NA** and **half pitch** (λ=193nm)

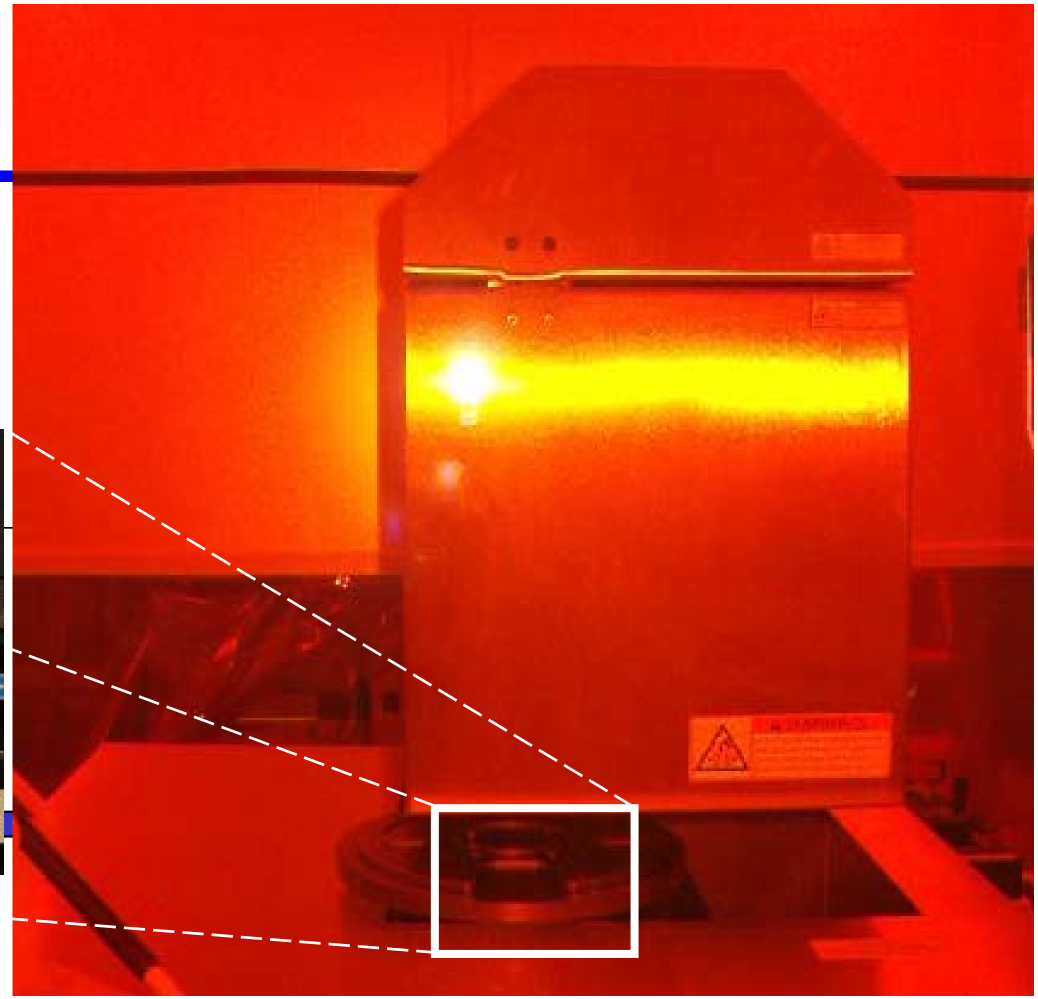


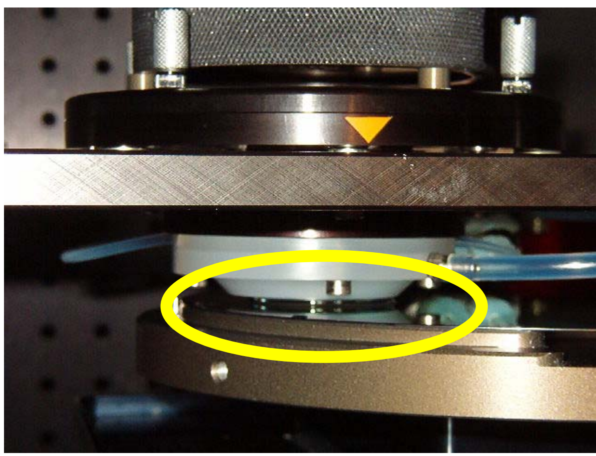
32nm half pitch limit requires **1.65 NA**

193nm immersion lithography
Liquids beyond water?

High index liquid testing on ASML Immersion Interference Printer

Excimer laser





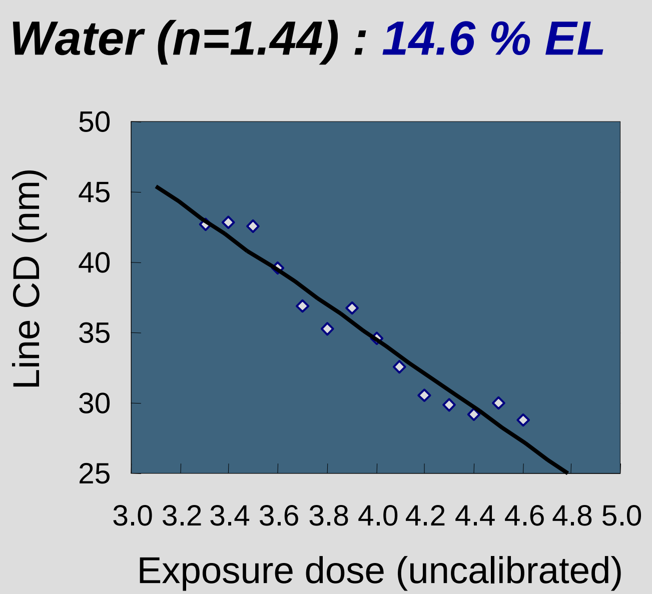
HIL stays between prism and wafer during stage motion

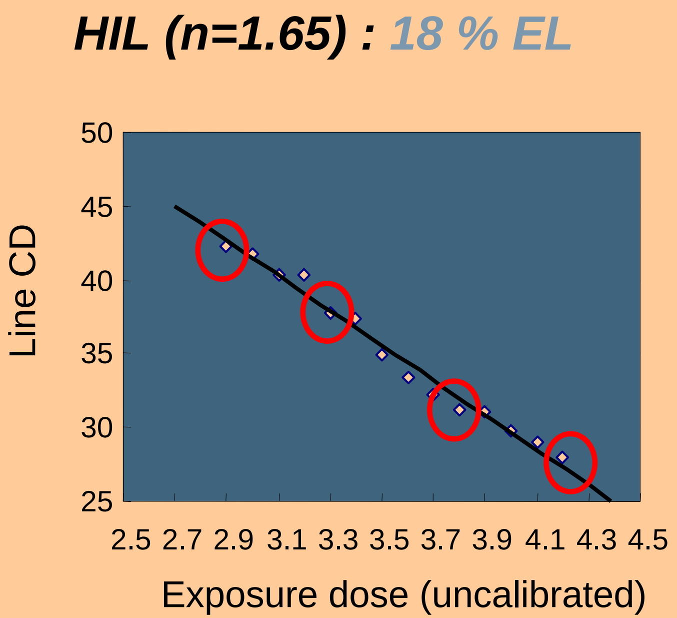
Stages

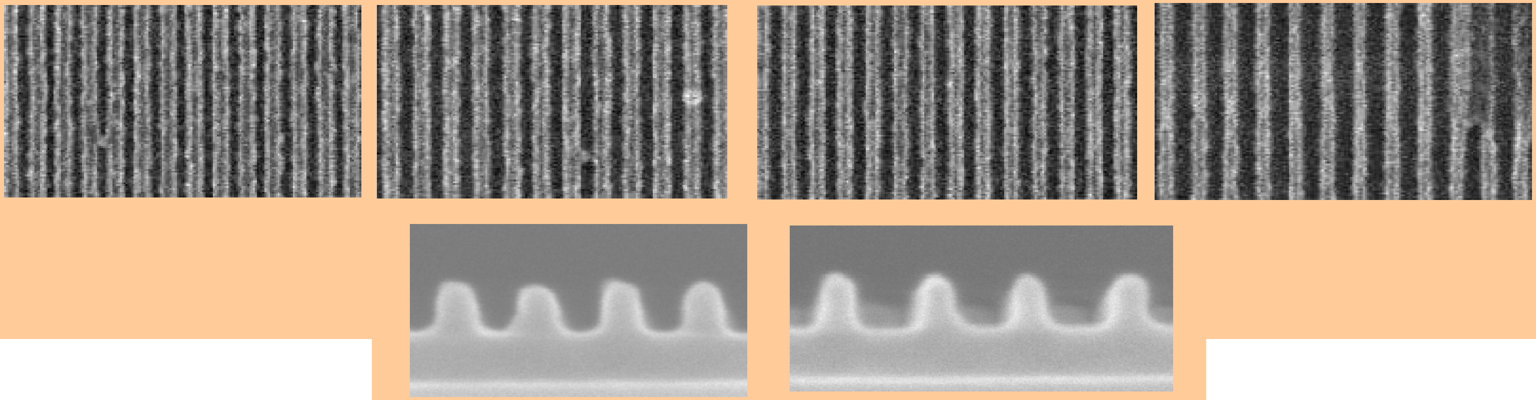
193nm immersion lithography

Outlook high index liquids

- Lithographic results 2nd generation fluids (n=1.65) :36nm HP

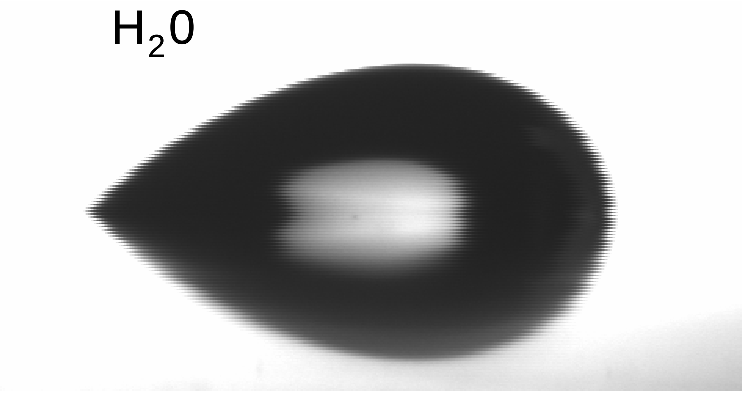






Contact angle measurements

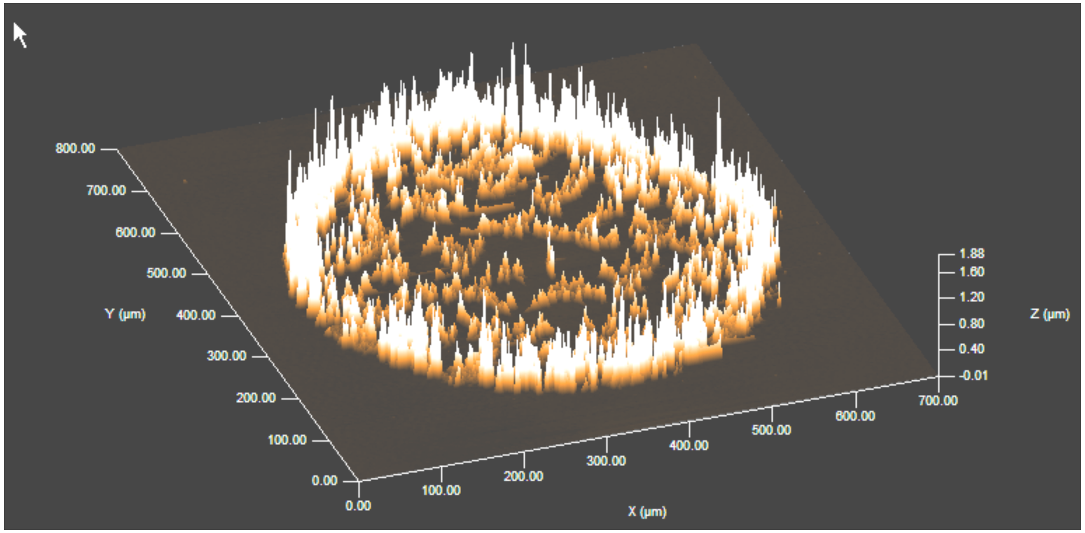
- Much lower surface tension : containment ?

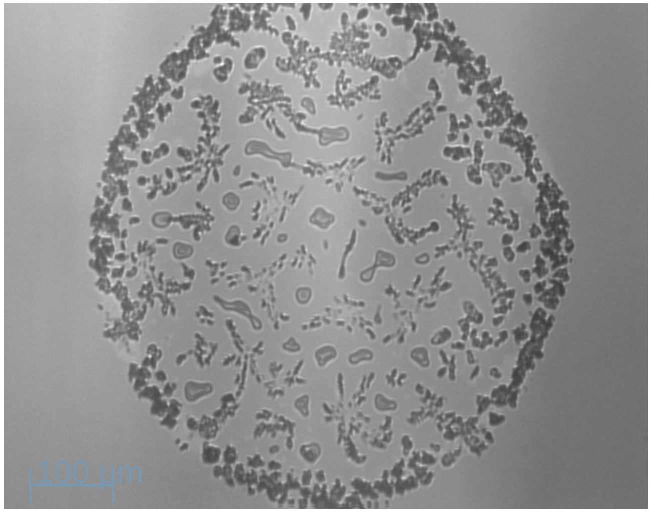


2nd generation HI liquids

Interaction HI liquid with resist (defect formation ?)

- Purpose:
  - apply droplets of the liquid on either an inert substrate or resist surface in a controlled way
  - Analyse what is left after drying (profilometry)





NA=1.65 requirements

application

- **High n_f Resist development** — imaging characterization, defectivity
- **High n_f Fluid characterization (n_f>1.9)** — Defectvity: Leaching & drying stains

Can we use HI fluids?

immersion system

- **Fluid recycling system** — Radiation & contamination evaluation
- **Fluid containment** — Scanning tests & IH evaluation

Can we make the system?

lens

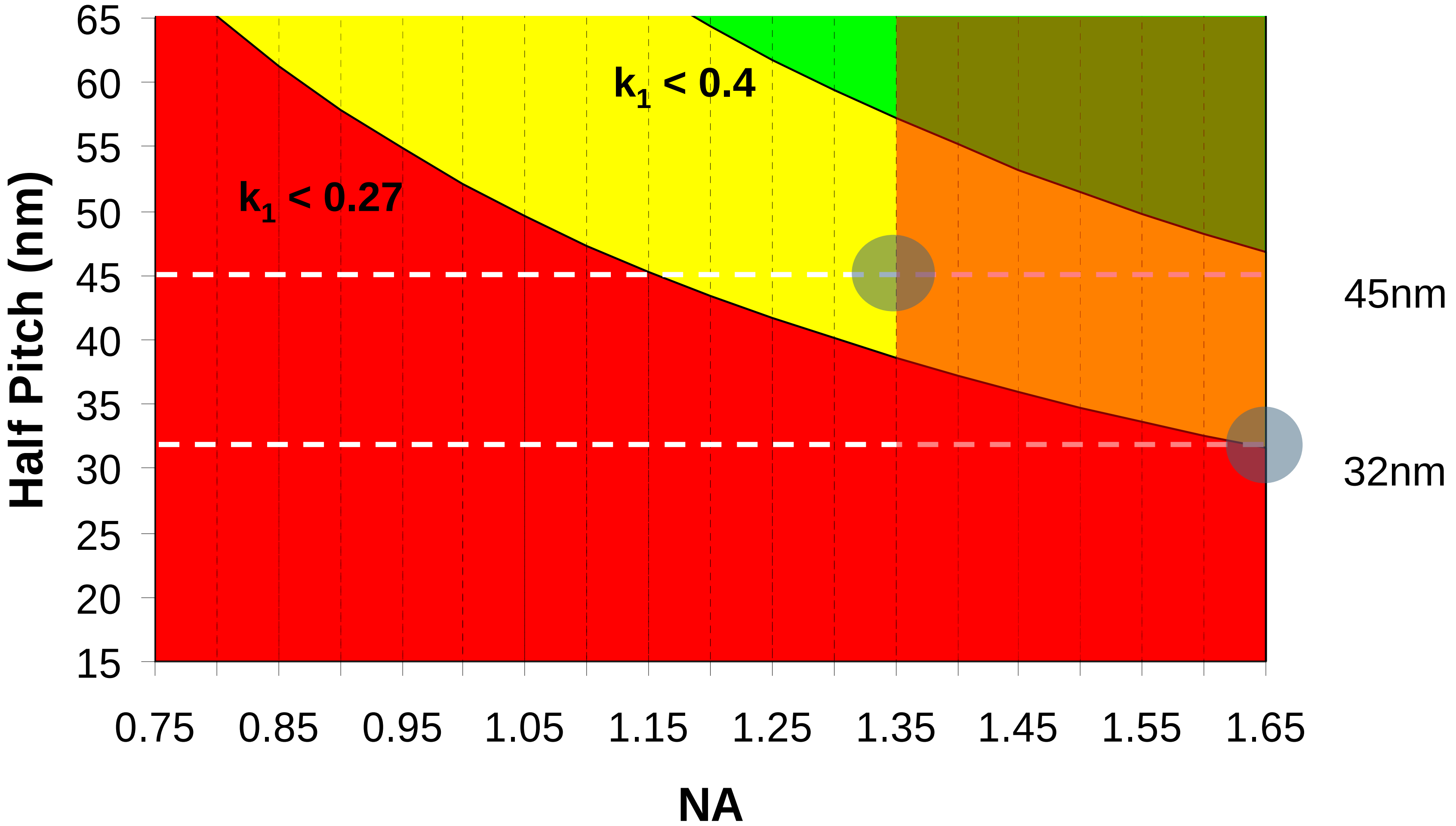
- **Optical system** — HRI glass evaluation (n_f > 1.8)

Can we make the lens?

TIMING is most critical

193nm immersion lithography
Ultimate limits

- **k_1** as function of **NA** and **half pitch** (λ=193nm)



Outline

- Introduction
- 193 nm immersion lithography
- EUV Lithography
- Double patterning
- Conclusions

- 2005 International Symposium on EUVL

Critical Technical Issues for EUV Lithography

Top 3 Critical Issues	2004 Rank
1. Resist resolution, sensitivity and LER	3
2. Collector lifetime	2
3. Availability of defect free masks	1
4. Source power	

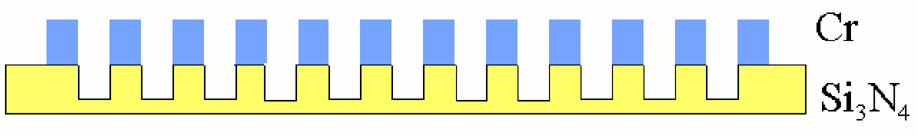
Remaining Critical Issues

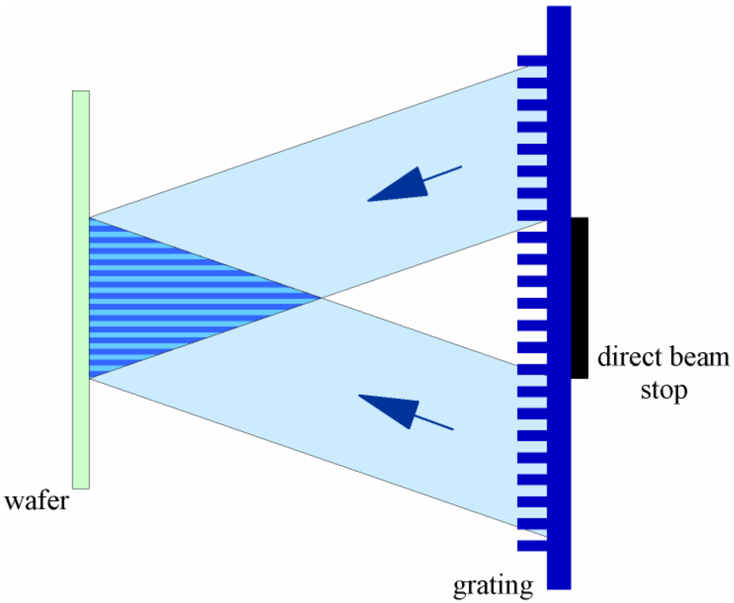
- Reticle protection during storage, handling and use
- Projection and illuminator optics quality and lifetime

*** Significant concern: Timing and cost / business case for EUVL development.

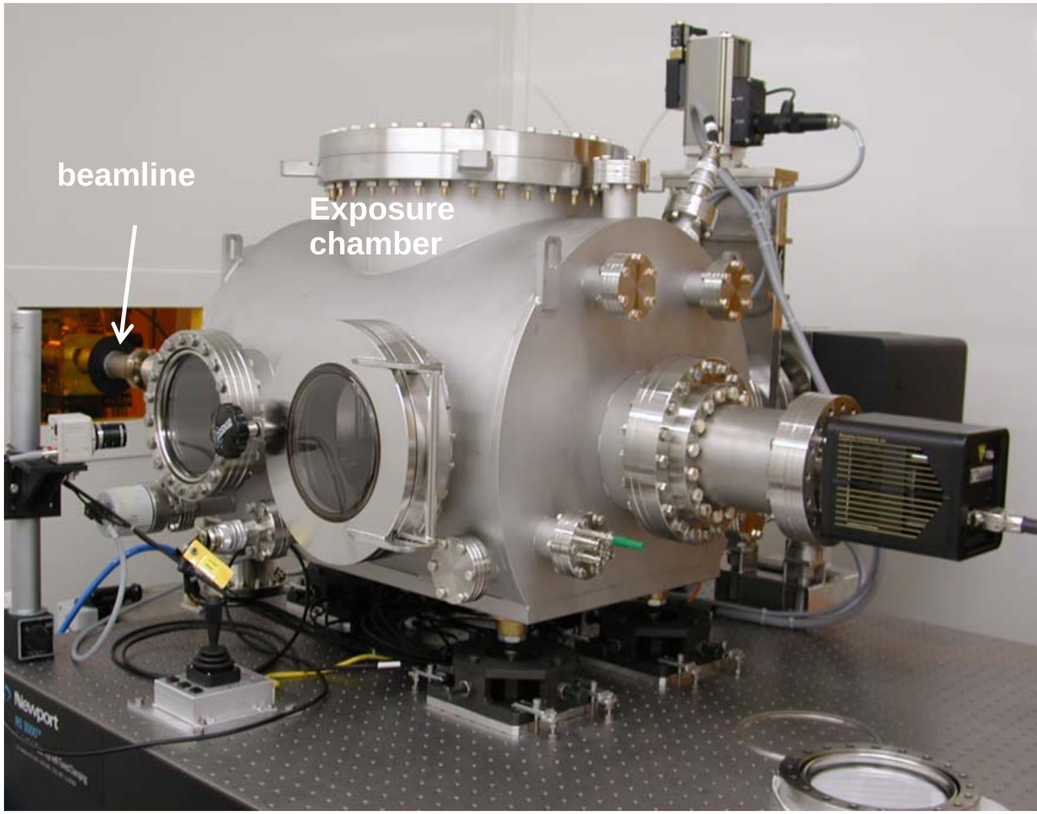
Experimental : Interference Lithography
Paul Scherrer Institute (PSI), Switzerland

Mask:

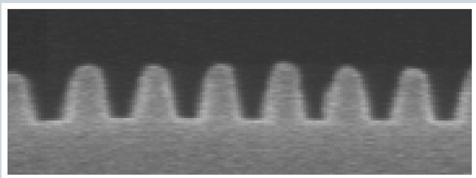
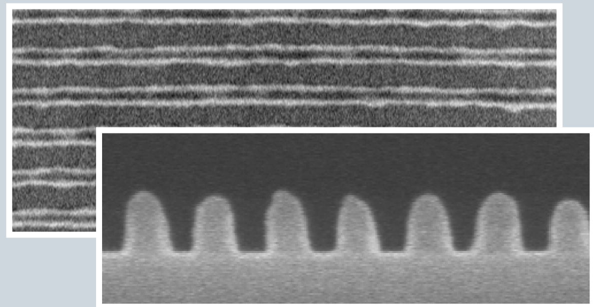
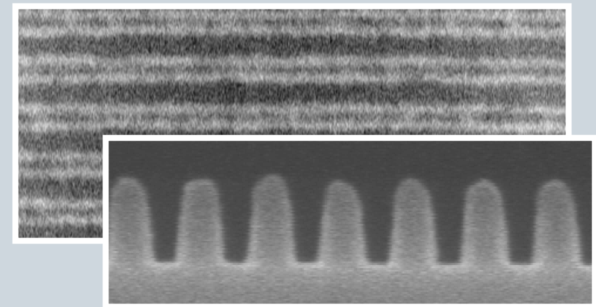
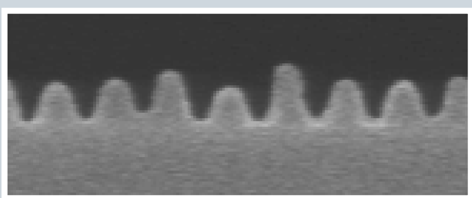
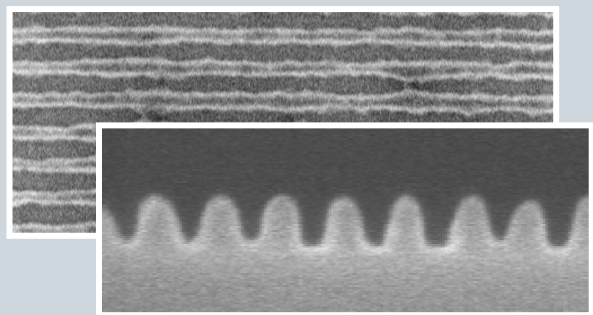
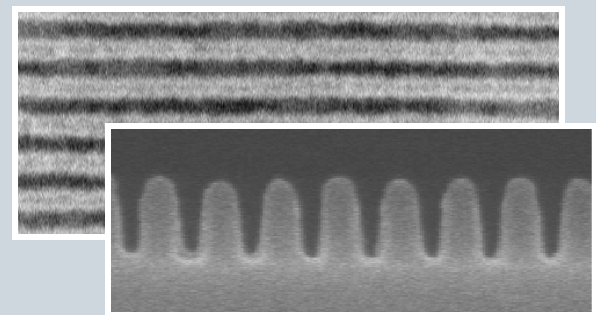
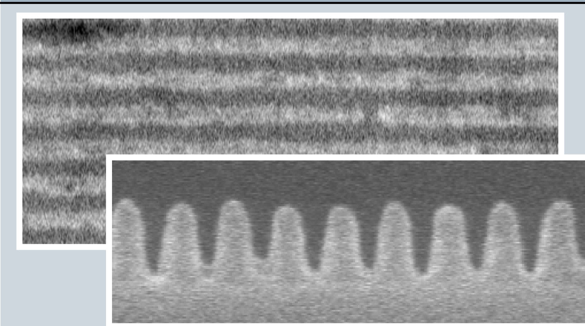




$$P_{wafer} = \frac{P_{mask}}{2}$$

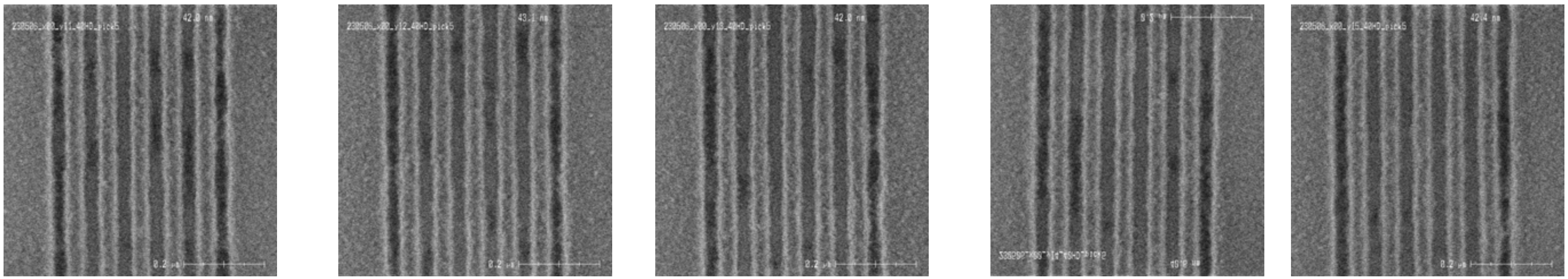


EUV Resist progress

	2004	2005	2006
40 nm			
32.5 nm			
30 nm			
	20 mJ/cm²	7.5 mJ/cm²	12.4 mJ/cm²

AD-tool imaging results :
40nm scanning H-lines/spaces 'through focus'

40nm L/S



-100 nm | -50 nm | near focus | +50 nm | +100 nm

>200 nm DOF

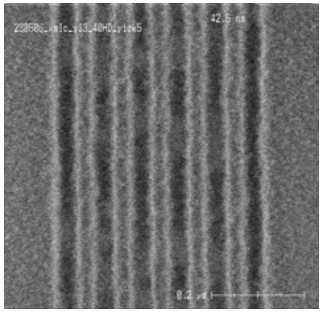
Resist: MET-2D
~18 mJ/cm2
NA=0.25, σ=0.5
no process optimization yet

AD-Tool imaging results :
40nm scanning H-lines/spaces ‘through slit’

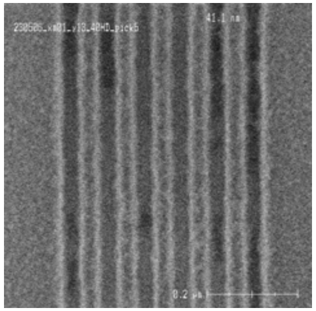
(22-May-’06)

Full slit coverage

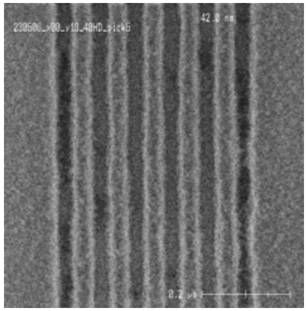
40nm L/S



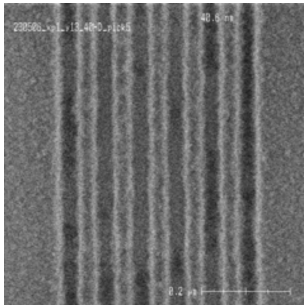
-10.6 mm



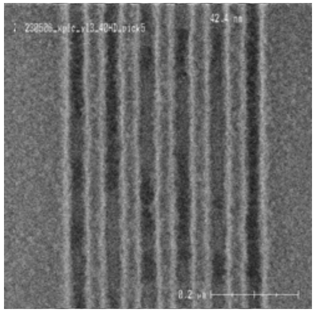
-6.36 mm



0.0 mm



6.36 mm

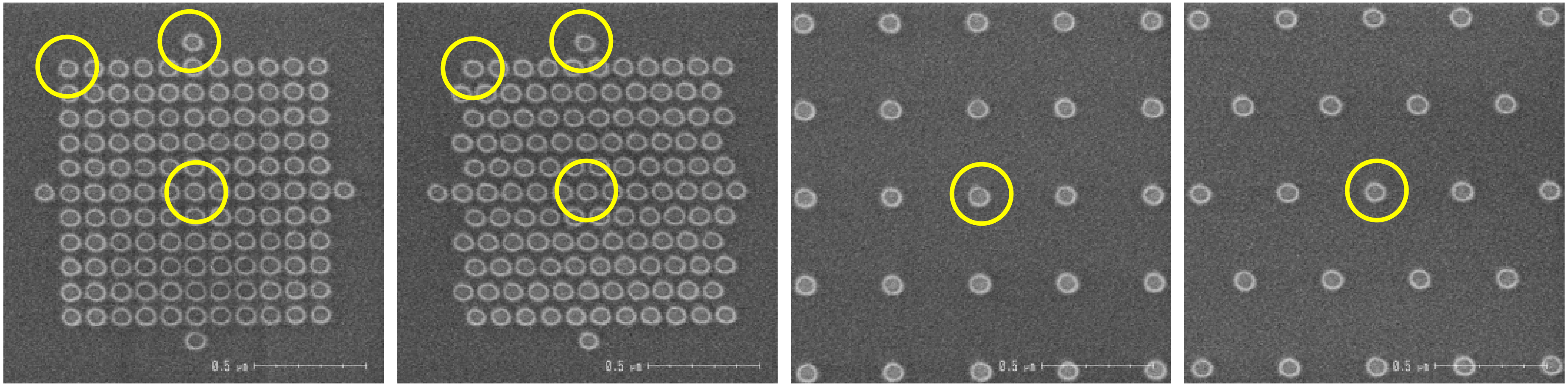


10.6 mm

Resist: MET-2D
~18 mJ/cm2
NA=0.25, σ=0.5
no process optimization yet

AD imaging results: 55 nm CH

Dense (aligned) | Dense (staggered) | Iso (aligned) | Iso (staggered)



All at same conditions:

- NA/Illumination/focus/dose
- Binary mask
- No OPC applied!

55 nm CH

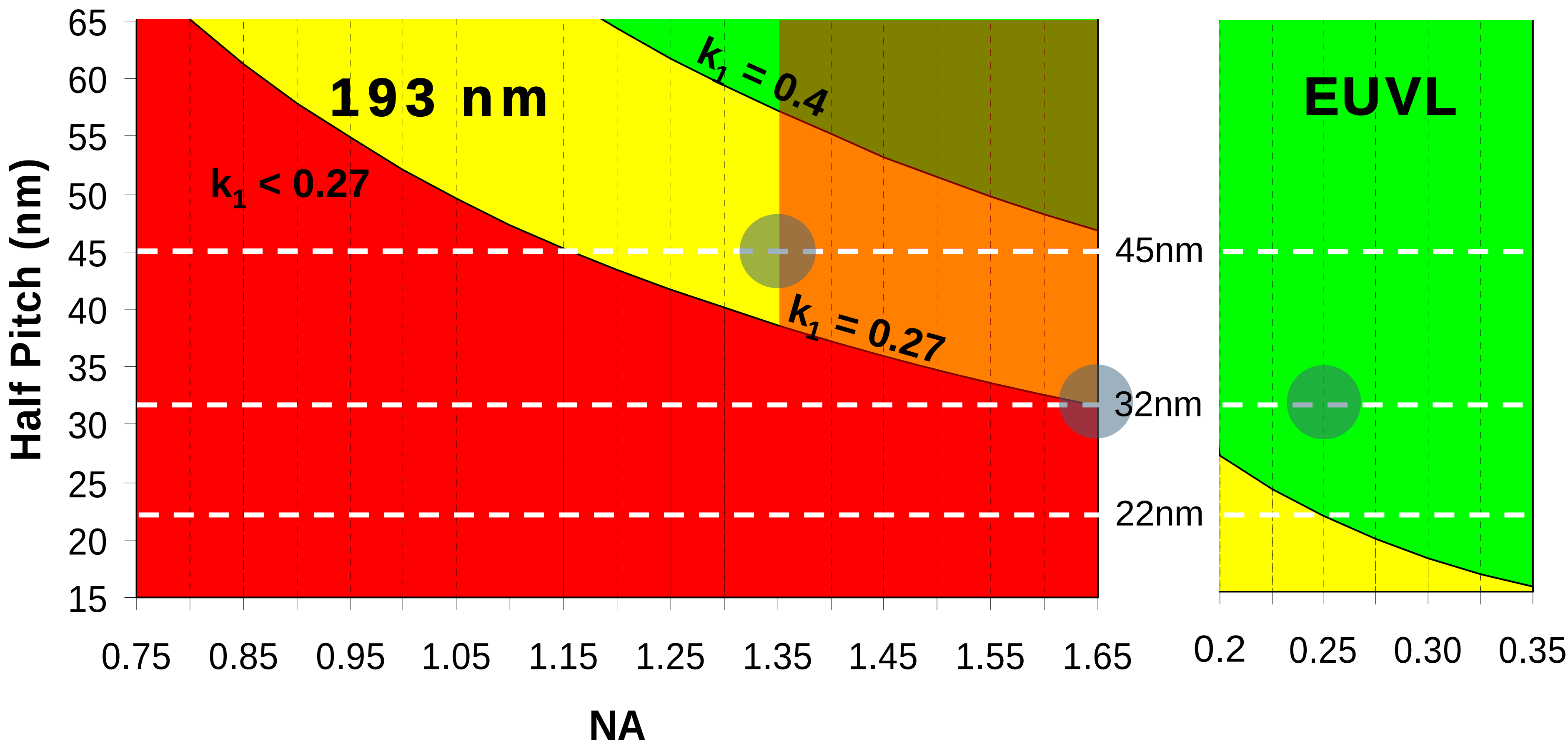
Resist: MET-2D
no process optimization

~40 mJ/cm^2

NA=0.25, σ=0.5

Double patterning
Outlook

- k_1 as function of **NA** and **half pitch** (λ=193nm)

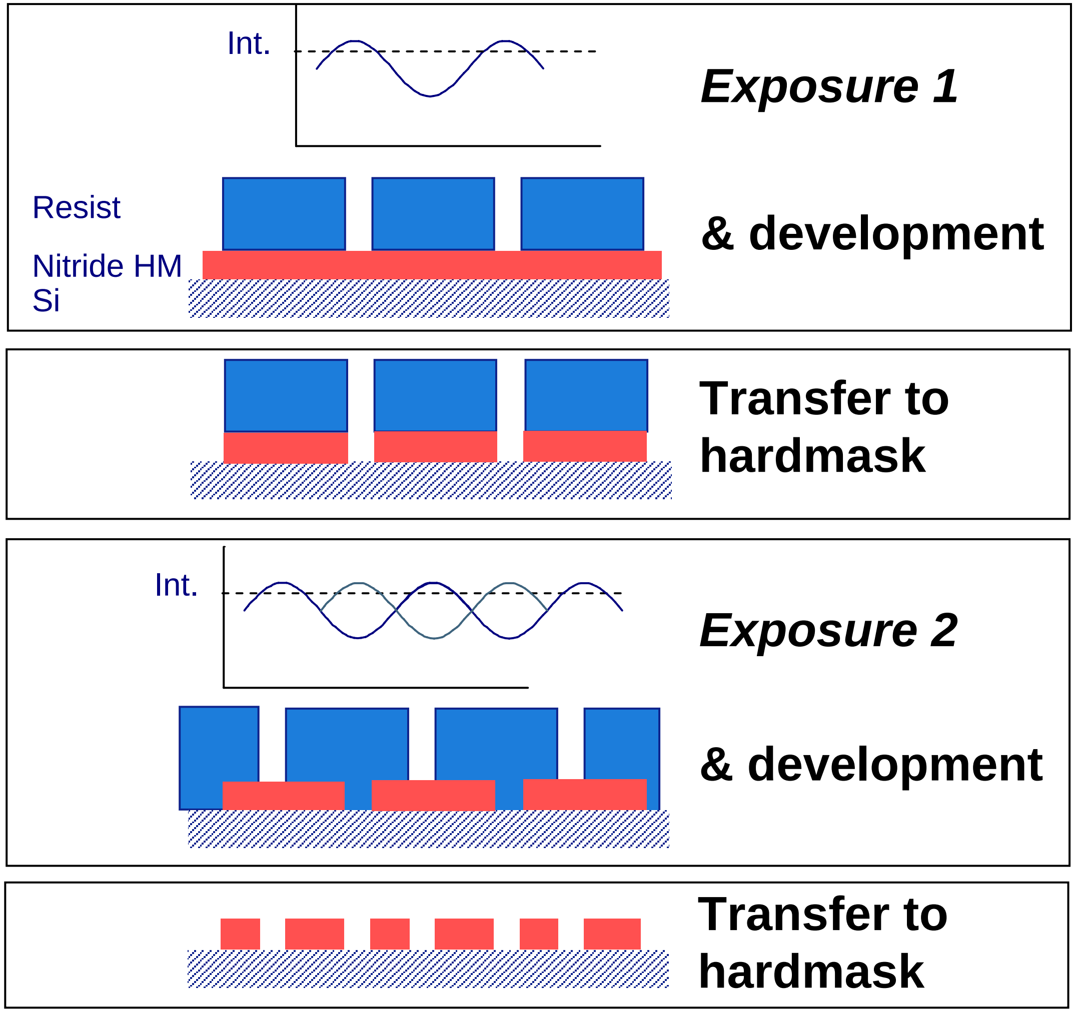


Outline

- Introduction
- 193 nm immersion lithography
- EUV Lithography
- Double patterning
- Conclusions

Double patterning (2x litho + 2x etch)

Possible integration flow



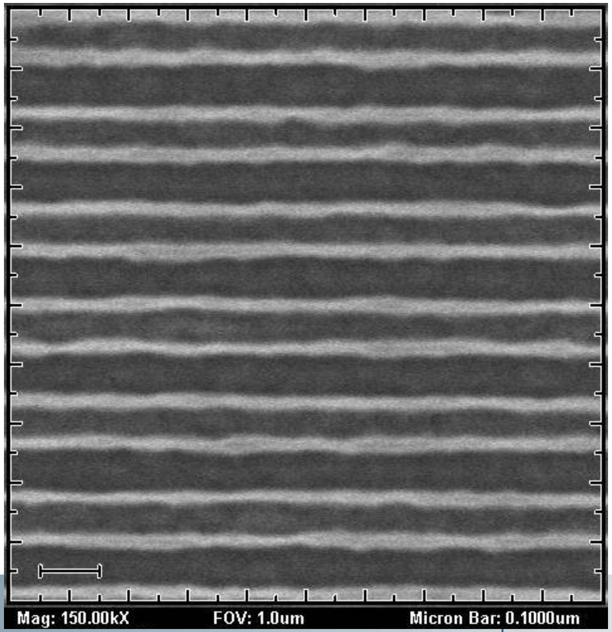
1nm alignment error -> 1nm CD change

ASML XT:1400
0.93 NA

40 nm L&S

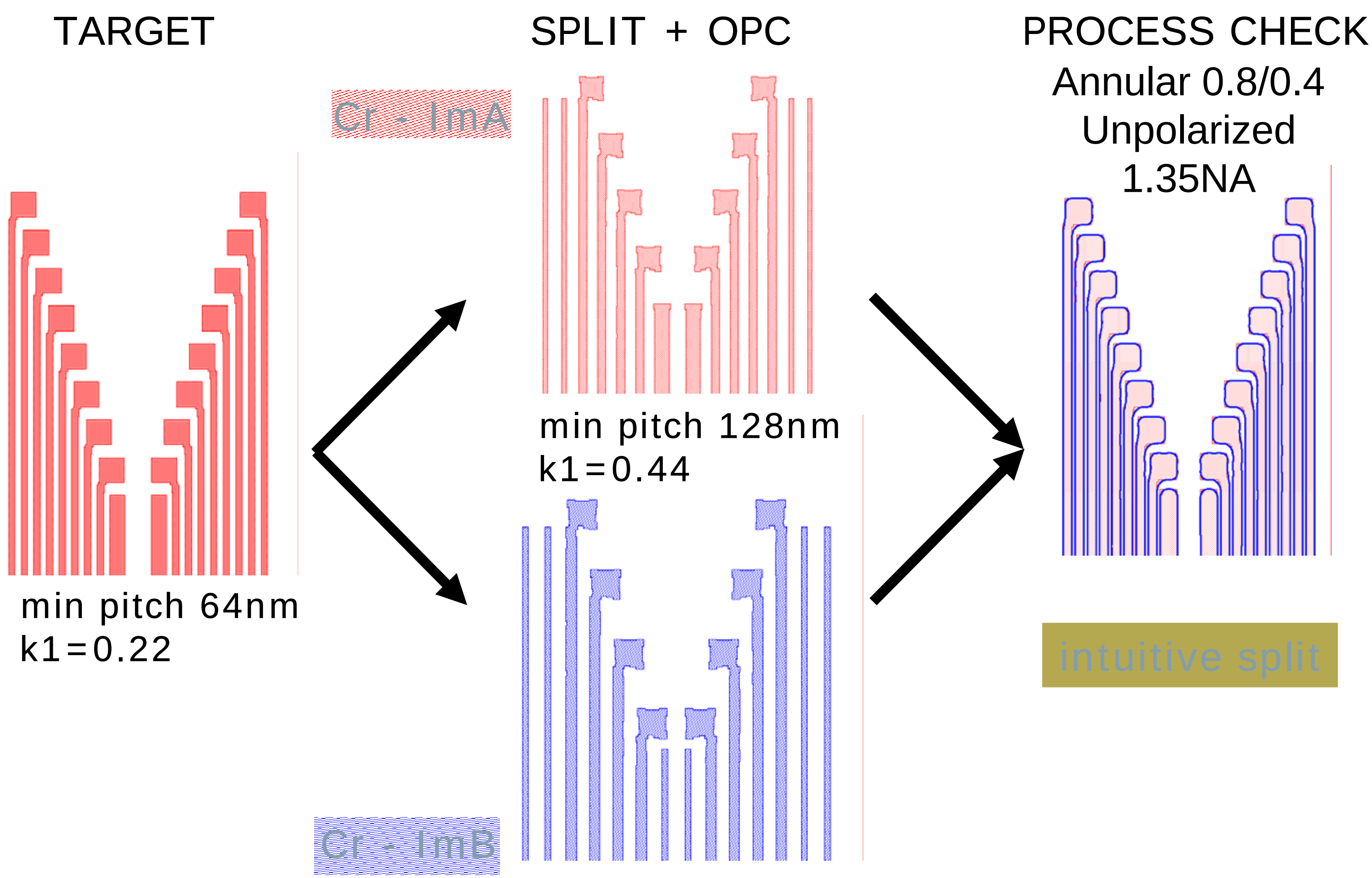
etched in oxide hard mask on poly-Si

k_1=0.19



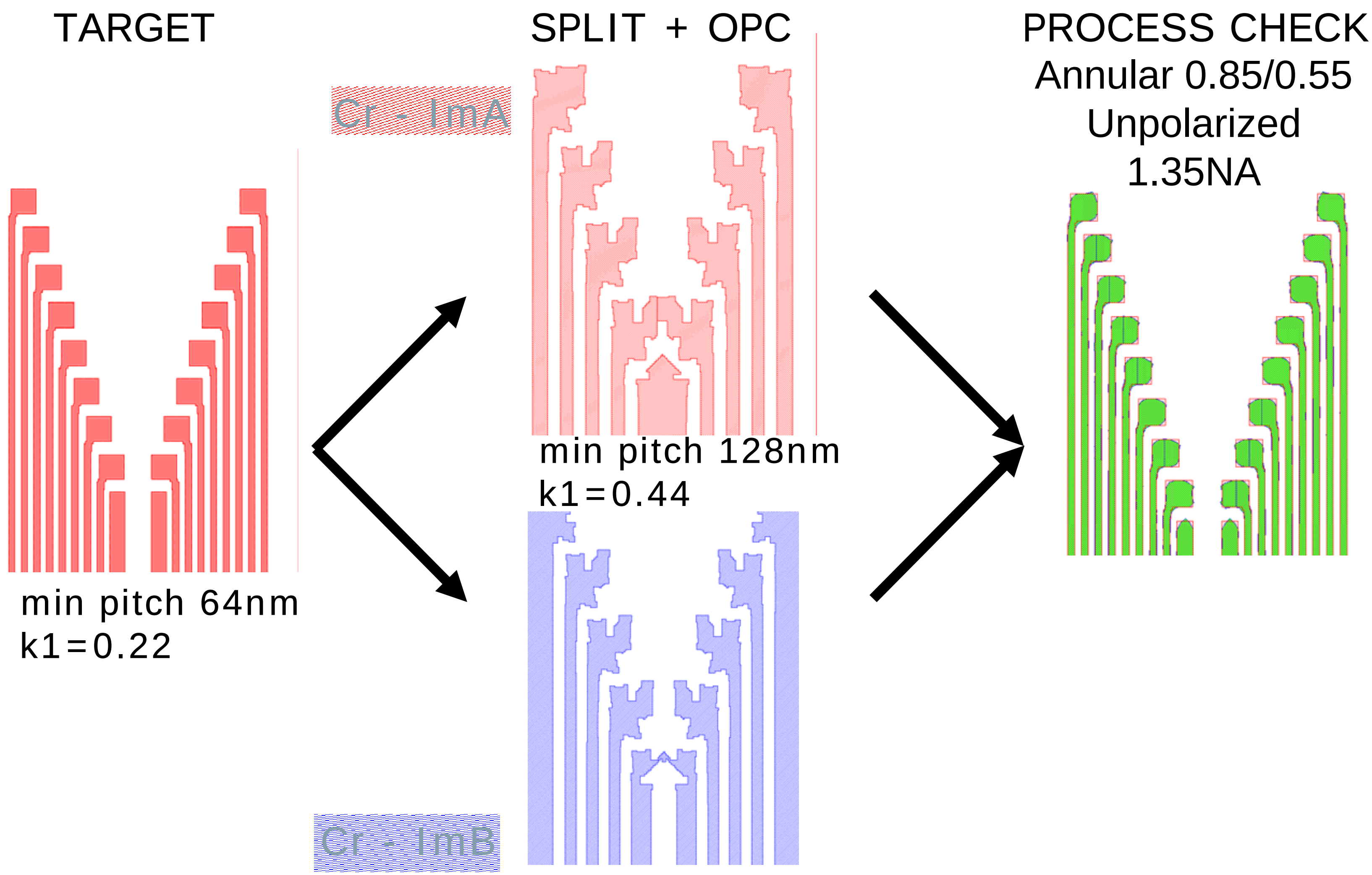
Design Split exercises NAND FLASH

Double Line for Poly



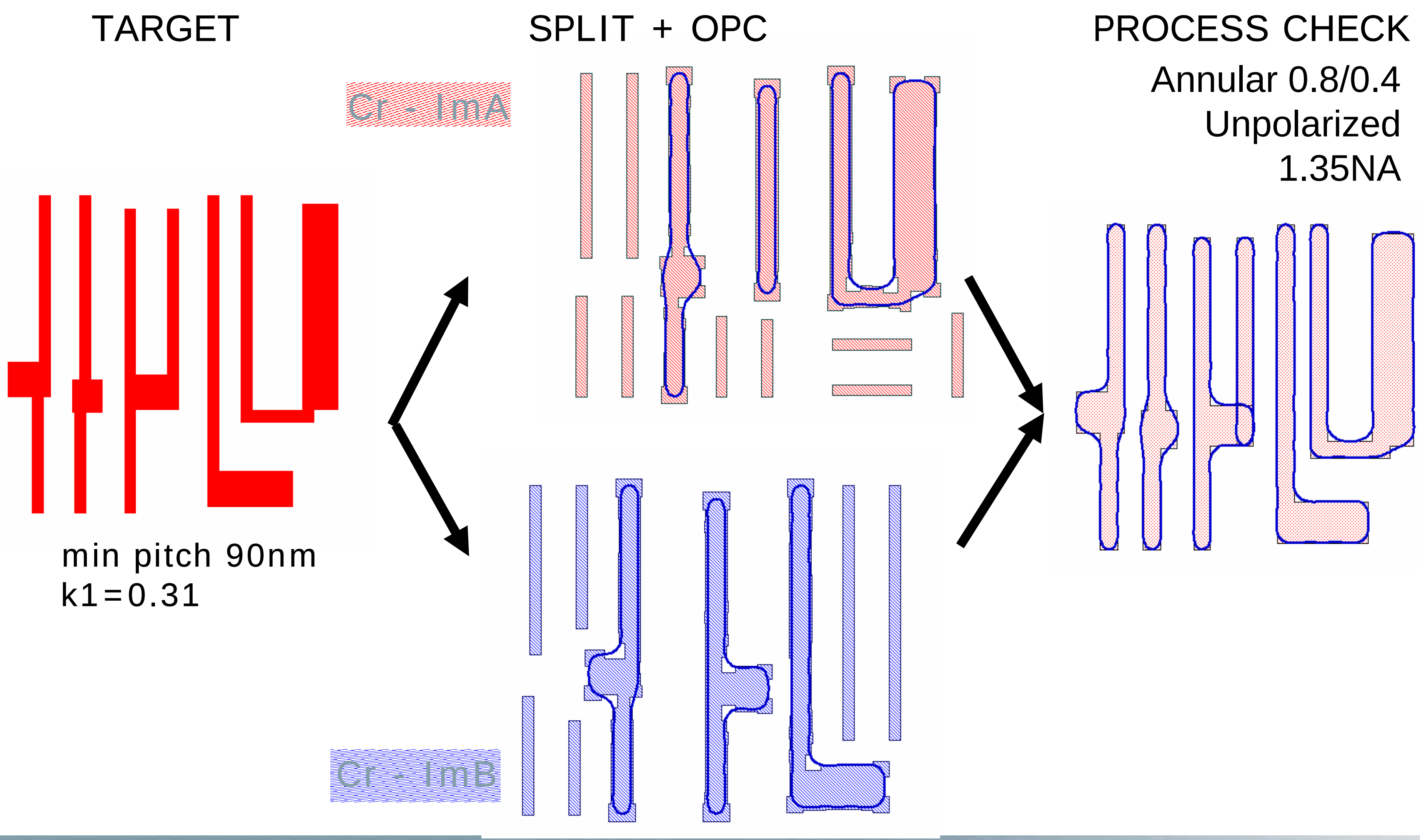
Design Split exercises NAND FLASH

Double Trench for Poly



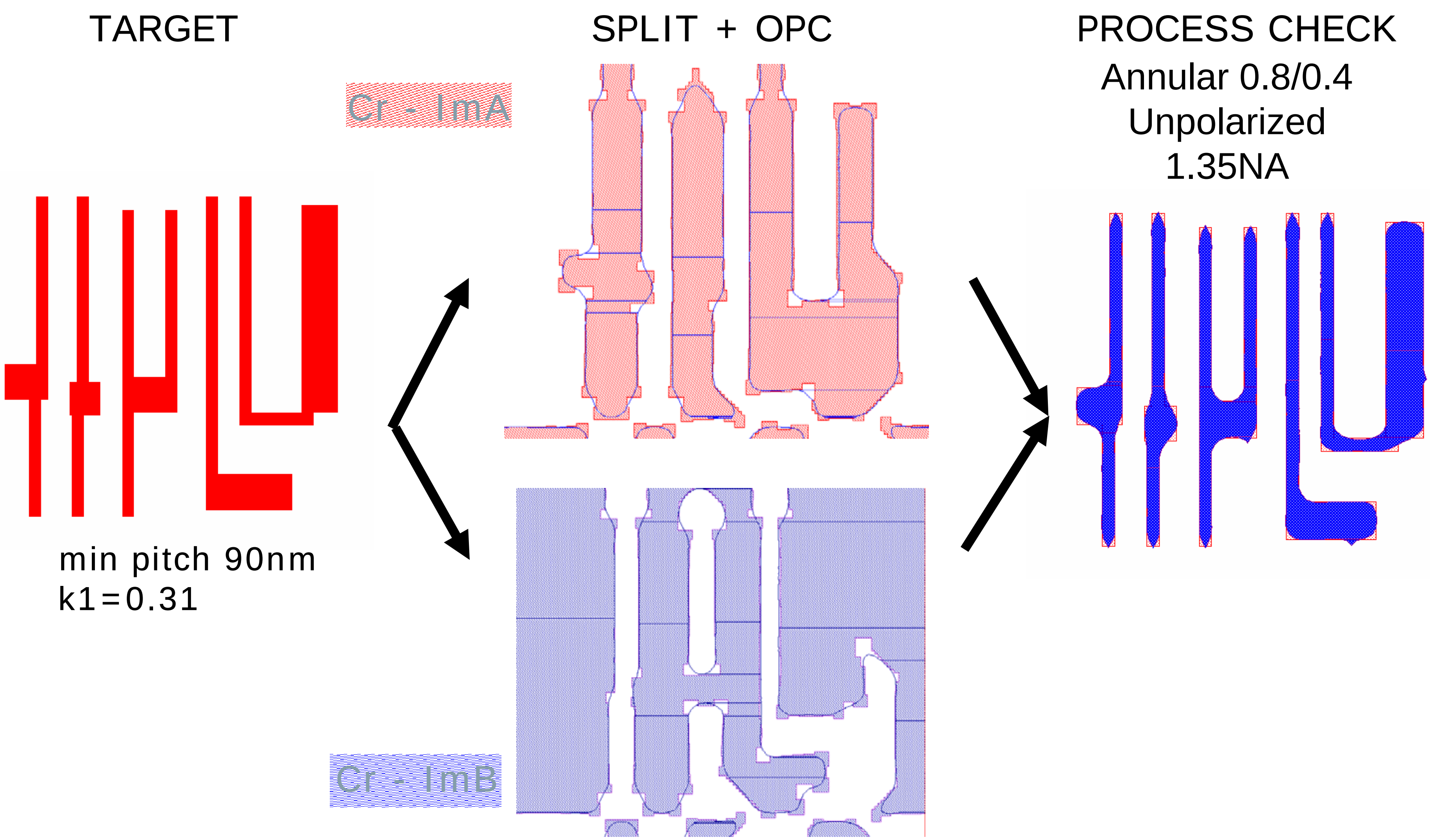
Design Split exercises Logic NOR

Double Line for Poly



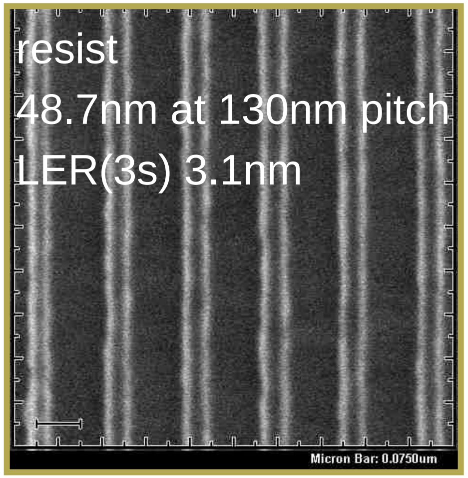
Design Split exercises Logic NOR

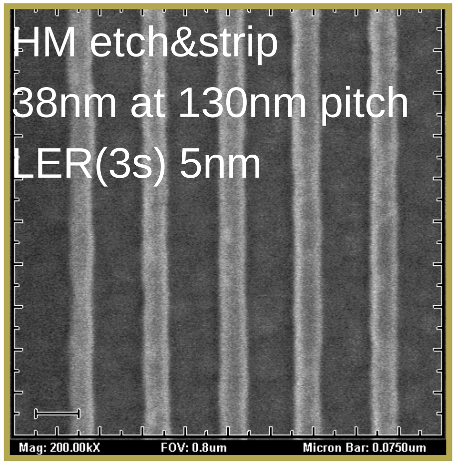
Double Trench for Poly

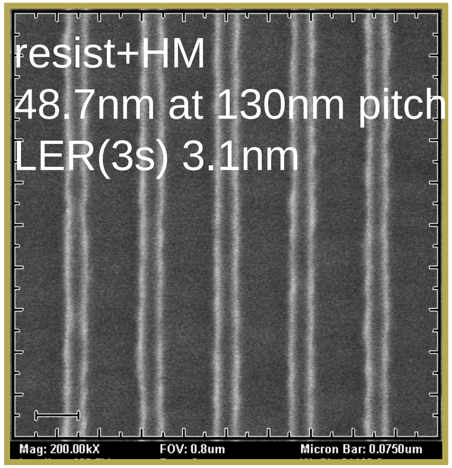


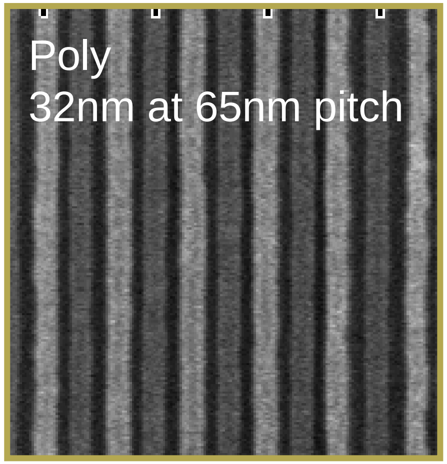
Double Line for Poly
DP k1=0.14

/1250i – 193nm
0.85NA – Dipole
DP 32nm 1:1

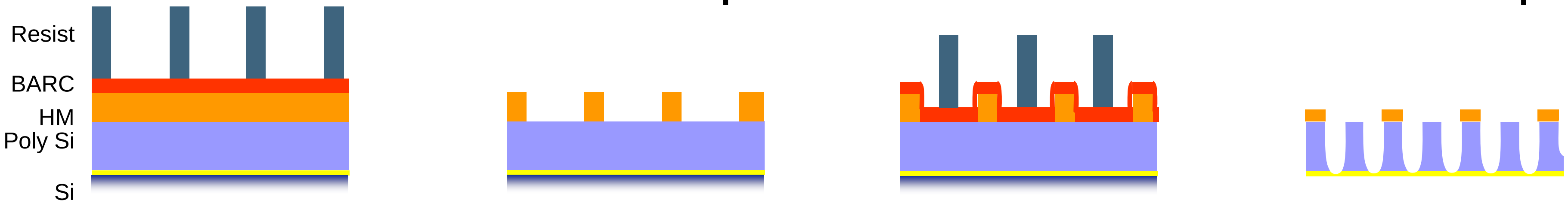




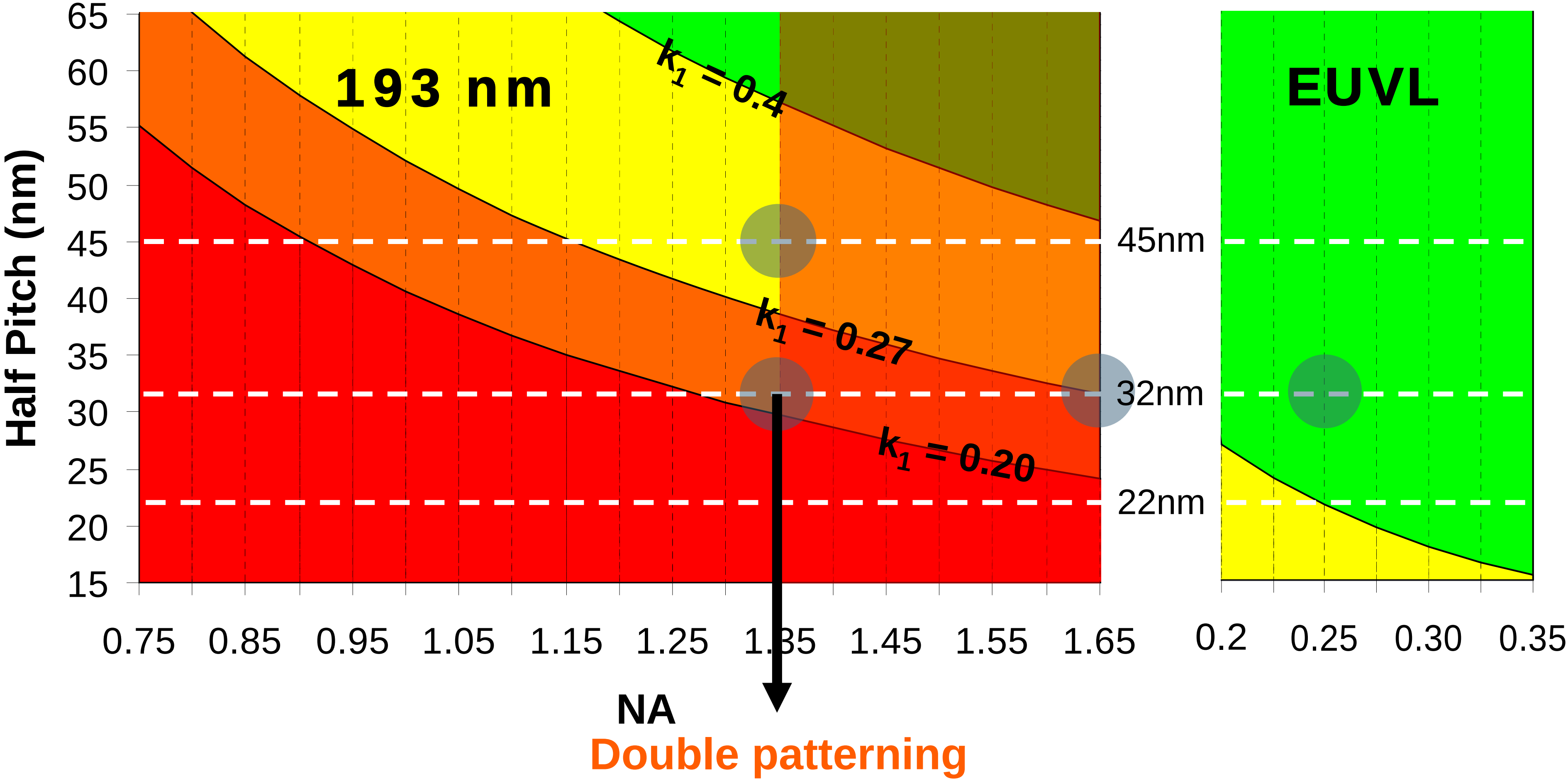




Litho | Etch/strip | Litho | Etch/strip



- **k_1** as function of **NA** and **half pitch** (λ=193nm)



Double patterning
Outlook

- **Lowest risk route to 32nm half pitch in time**
- **But… worst in terms of CoO**
  - Requires 2 critical masks per critical layer
  - Reduces throughput (~ factor 2)
  - Adds cost of second etch step
  - Impacts total cycle time (additional photo, etch, …)
  - Some integration approaches very critical for alignment
- **Any development improving CoO issues is a plus for double patterning**

Outline

- Introduction
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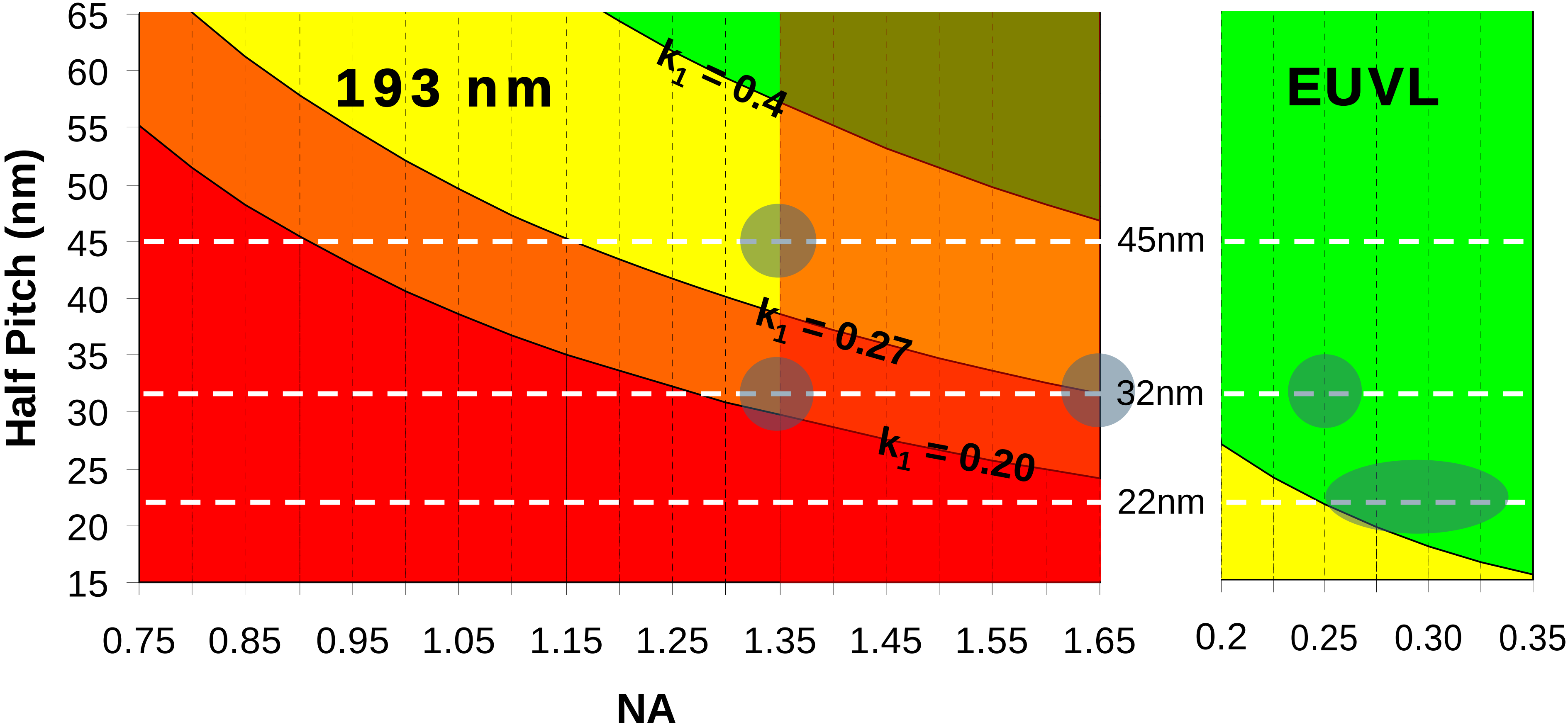
Summary and conclusions

- Still 3 lithography options for 32nm half pitch critical levels
- Immersion lithography beyond water urgently needs a 3rd generation fluid (n>1.8) to be identified
- EUV lithography makes steady progress
  - First ASML EUV alpha demo tools about ready to ship to the field
  - EUV resist has become issue number one and requires a lot of focus
  - EUVL is the solution for small contact holes !
- Double patterning is the lowest-risk route towards 32nm but CoO needs to be controlled
- Towards 22nm volume production, EUVL is the only option

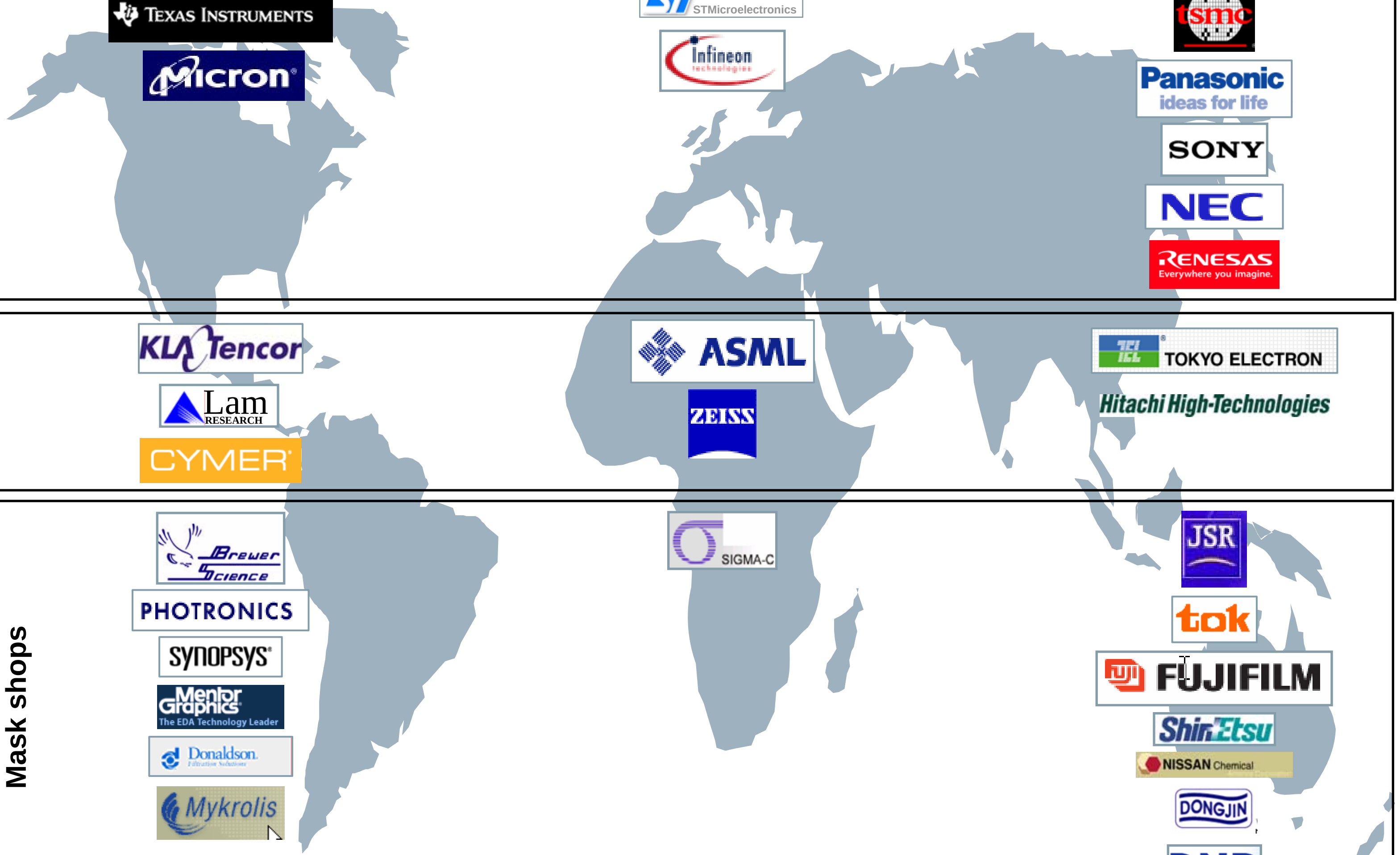
Double patterning

Outlook

- **k₁** as function of **NA** and **half pitch** (λ=193nm)



Aknowledgements



IC companies

- Intel
- Texas Instruments
- Micron
- Philips
- STMicroelectronics
- Infineon technologies
- Samsung
- tsmc
- Panasonic ideas for life
- Sony
- NEC
- Renesas Everywhere you imagine.

Equipment Suppliers

- KLA Tencor
- Lam Research
- Cymer
- ASML
- Zeiss
- Tokyo Electron
- Hitachi High-Technologies

Material Suppliers Software Suppliers Mask shops

- Brewer Science
- Photronics
- Synopsys
- Mentor Graphics The EDA Technology Leader
- Donaldson
- Mykrolis
- SIGMA-C
- JSR
- tok
- Fujifilm
- Shin-Etsu
- Nissan Chemical
- Dongjin
- DNP
- Toppan
- Hoya

The world's largest 193nm immersion lithography effort

aspire invent achieve

Thank you!

imec

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