High Throughput Maskless Lithography

Sokudo lithography breakfast forum

July 14th 2010

Bert Jan Kampherbeek, VP Market Development and co-founder

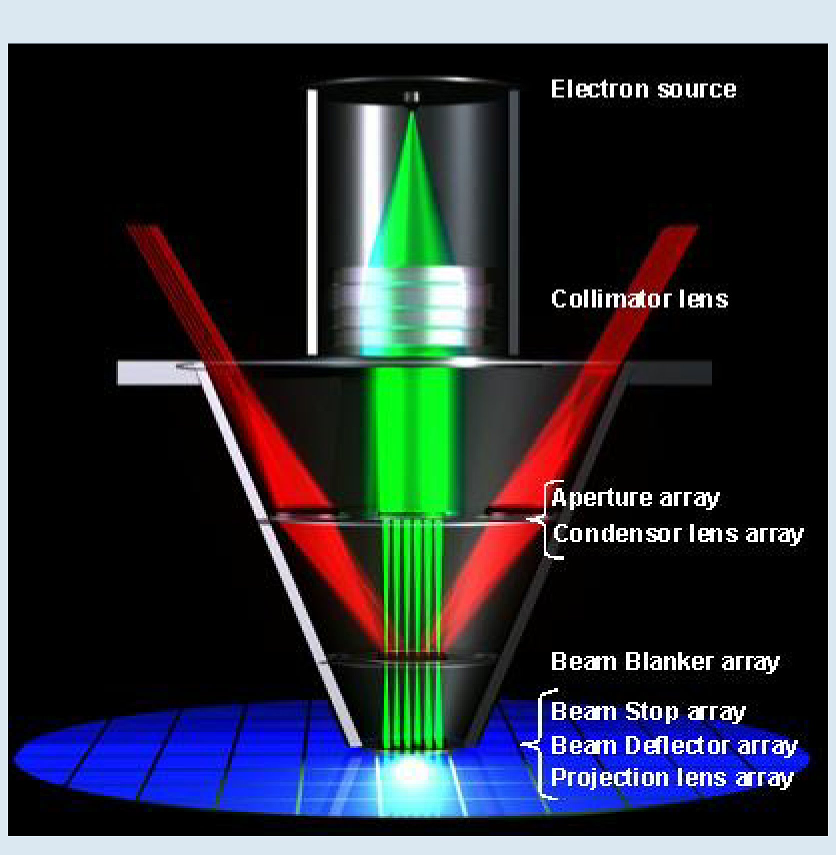
Agenda

- MAPPER's Objective
- MAPPER's Status
- MAPPER's Roadmap

MAPPER's objective: Provide lithography solution for 32 nm hp and beyond

- Provide 10 wph lithography unit in ~ 1 m^2 per unit at a competitive price
- Cluster several 10 wph units together, for example 10 units for 100 wph
- Application of first generation MAPPER manufacturing machines:
  - Contact and via layers, 32 nm hp (22nm logic node)
  - Metal layers, 32 nm hp
  - Cutting / filling layers in double patterning, 16 nm hp (11nm logic node)
- MAPPER solution is extendable to at least:
  - 16 nm hp random patterning @ 10 wph in 1 m^2
  - 8 nm hp with pitch division and cut/fill @ 10 wph in 1 m^2

MAPPER builds a system with 13,000 parallel electron beams for 10 wph



Key numbers 22nm node:

	HVM	pre-alpha
#beams and data channels	13,000	110
Spotsize:	25 nm	35 nm
Beam current:	13 nA	0.3 nA
Datarate/channel	3.5 Gbs	20 MHz
Acceleration voltage	5 kV	5 kV
Nominal dose	30 $\mu C/cm^2$	30 $\mu C/cm^2$
Throughput @ nominal dose	10 wph	0.002 wph
Pixel size @ nominal dose	3.5nm	2.25 nm
Wafer movement	Scanning	Static

Tool cluster for 100 wph

MAPPER single column tool. Upgrade to 13,000 beam for 10WPH

Application for MAPPER's technology (Logic example)

Assuming four critical metal layers at 22 nm:

	Direct patterning	Cutting	Position w.r.t. ArFi
Gate layer		X	Complementary
Contact layer	X		Alternative
Metal 1	X	X	Complementary
Via 1	X		Alternative
Metal 2	X	X	Complementary
Via 2	X		Alternative
Metal 3	X	X	Complementary
Via 3	X		Alternative
Metal 4	X	X	Complementary
Via 4	X		Alternative

Applicable to at least 10 critical layers

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Overview current MAPPER machine

- 1.3 x 1.3 m footprint containing 300 mm wafer stage
- Electron optics is completely in vacuum
  - Source used for CRT application
  - Lens arrays manufactured with MEMS techniques
- Wafer stage is in vacuum
  - Long stroke motors outside shielding
  - Short stroke magnetically shielded
- Data path is in the sub-fab (not in picture)
  - Blanker chip with integrated photodiodes switches electron beams
  - Data path connected through fibers with electron optics

Two tools shipped for enabling infrastructure development

Tool: AST-S005
Location: Delft

Tool: AST-S004
Location: Grenoble

Tool: AST-S006
Location: Hsinchu

Results of MAPPER prototype tool @ TSMC (1/2)

C/H Resolution by p-CAR

1. CAR-B / C are the lower sensitivity versions of A, while keeping similar contrast.
2. CAR-C is designed for higher resolution.
3. CH @ 30nm HP were constantly resolved by good resist samples.

	CAR-A	CAR-B	CAR-C
C/H HP30 Image			
Dosage (μC/cm²)	36.8	48.3	44
Average CD (nm)	32.5	34.2	31.2

Jack Chen, June 21, 2010, IMAGINE Review, Grenoble

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Results of MAPPER prototype tool @ TSMC (2/2)

L/S Resolution by p-CAR

HP30 / Dose15

Baseline CAR

- New CAR sample has a 1/3x lower sensitivity than baseline
- CAR thickness: 45nm
- Raster scan@ 2.25nm pixel, spot size ~40nm, beam current ~185pA
- Large biasing was required to resolve L/S at HP30, with different biasing for each pitch.
- Further process optimization ongoing.

HP30 / Dose50 | *HP32 / Dose50* | *HP36 / Dose50* | *HP45 / Dose50*

Modified CAR

LWR ~ 15nm

Jack Chen, June 21, 2010, IMAGINE Review, Grenoble

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Results of MAPPER prototype tool @ CEA-Leti (1/4)

leti
MAPPER

Status of the IMAGINE partnership

Infrastructure partnership

tok
DOW
aselta
SOKUDO

LETI

imagine

IMAGINE partners

tsmc
ST

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cea

Results of MAPPER prototype tool @ CEA-Leti (2/4)

Coat/Develop Track supporting

Results of MAPPER prototype tool @ CEA-Leti (3/4)

32nm hp resolution

- HSQ negative resist

Pitch 65nm
CD=26nm
D=673µC/cm²

- Positive tone CAR

Pitch 65nm
CD=37nm
D=42µC/cm²

Pitch 80nm
CD=40nm
D=200µC/cm²

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Results of MAPPER prototype tool @ CEA-Leti (4/4)

leti

CAR-PRØ: Positive POR @ 5keV

Dense Line&Trench 32nm 1:1
CDmeas=37 nm

Semi-Iso Trench 32nm 1:10
CDmeas=36nm

CNT

SRAM22 from LETI

M1

Dense Contact 40nm 1:1
CDmeas=39.8 nm

Semi-Iso Contact 40nm 1:10
CDmeas=40 nm

23/03/2010 – IMAGINE workshop Tokyo | 44

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Key technical challenges in scaling towards 10 wph and HVM

		Pre-alpha status	HVM requirement	**Solution**
Data path	Pattern streaming	110 beams	13,000 beams	Bitmap input format and resampling
	Beam blanker	110 x 10 MHz	13,000 x 49 x 70 MHz	Ge photodiode in 65 nm CMOS
Electron Optics	Illumination optics	1.5 x 1.5 mm^2	26 x 26 mm^2	Conventional electrostatic optics
	Projection optics	25 nm spots over 1.5 x 1.5 mm^2	25 nm spots over 26 x 26 mm^2	Yield optimization and mechanical stabilization
	Contamination	40 ppm dose change per wafer (PMMA)	Same + plasma cleaning every ~ 1000 wafers	Plasma cleaning
Wafer positioning	Thermal stability	1 s	360 s, 1 wafer exposure	MAPPER proprietary
	Position stability	50 nm	1 nm	Interferometer control and EMC reductions
Infrastructure	Process (resist)	40 nm in PMMA (60 uC/cm2) and HSQ (100 uc/cm2)	30 nm in 'industrial resist' @ 30 uC/cm2	Test available resists for EUV
	Data preparation	Proximity correction verified by simulation	Proximity correction verified in resist	Leti + TSMC tools to verify assumptions

Conclusions

- MAPPER's technology provides a 10 wph system on a 1 m^2 footprint at low cost
- MAPPER's technology is an alternative for both direct patterning and pitch splitting with cutting and filling, this makes the technology viable for > 10 critical layers / chip
- MAPPER has installed two machines in the field, one at TSMC and one at CEA – Leti
- Both machines, designed for 45 nm hp resolution, resolve ~ 30 nm hp in CAR
- At CEA-Leti a tool assessment and infrastructure program is ongoing: IMAGINE
- Solutions for scaling to 10 wph are available and are scalable for at least 3 generations
- In our opinion there are no fundamental roadblocks left

Thank you