Advanced Sub-20nm 450mm Lithography

Platform Maturity and Wafer Availability

Paul Hofemann
Corporate Marketing & Business Development

Molecular Imprints™
Corporate Profile

- **Global Nanoimprint Leader**
  - Headquartered in Austin, Texas
  - Installations and commercial partnerships established in semiconductor memory and HDD
  - DNP commercial imprint mask partnership
  - Eleven years experience and over $165 million invested

- **Strategic Objectives**
  1. Capture substantial share of the existing $6B semiconductor lithography equipment market
  2. Utilize MII’s low cost lithographic capability to enable new nanotechnology markets
Jet and Flash™ Imprint Lithography

**J-FIL™ Advantages**

- Sub-20nm Lithography with a Single Patterning Step
- Lowest Cost of Ownership
- Technology is Adaptable to Broad Applications
  - CMOS, Flat Panel Displays, Hard Disk Drives, Biotechnology, Clean Energy

With twelve years and $165M invested, there are 160 patents issued in US and 250 people working on J-FIL full-time around the world

- 1.5 picoliter resist jetting
- Precision mechanics
- Optimized takt times
- Sub-20nm mask
- Low cost replication
- Low defect
- High longevity
- Low viscosity
- 193-like resist performance
- Low particulates
- High adhesion to substrate

Molecular Imprints®
Jet and Flash™ Imprint Lithography (J-FIL™)

Proprietary, patented lithography technology with higher performance and lower cost than traditional optical products

Very High Resolution Nanoscale Patterning
- No wavelength of light imaging restrictions
- Room temperature process allows accurate overlay and high throughput

Low Cost of Equipment and Operation
- Significantly cheaper than optical lithography tools
  - No lens
  - No laser light sources
  - No tracks
  - No material wastage

Large Print Area
- Not limited by optical field sizes

Technology is Adaptable to a Variety of Applications
- Semiconductors
- Flat Panel Displays
- Hard Disk Drives
- HB-LEDs
- Biotechnology
- Clean Energy (Solar, Battery)
Key Market Opportunities

Semiconductor

Flat Panel Displays

Hard Disk Drives

- Memory ICs
- Wire Grid Polarizers
- Bit Patterned Media
# Semiconductor Platform Roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Equipment Partner</th>
<th>Imprint Modules</th>
<th>MII Systems</th>
<th>Mask Replication</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>(Multi-Modules Stepper System)</td>
<td>IM20</td>
<td>Imprio 300</td>
<td>3Xnm</td>
</tr>
<tr>
<td>2012</td>
<td></td>
<td>IM30</td>
<td>Imprio 450</td>
<td>2Xnm</td>
</tr>
<tr>
<td>2013</td>
<td></td>
<td></td>
<td></td>
<td>1Xnm</td>
</tr>
<tr>
<td>2014</td>
<td></td>
<td></td>
<td></td>
<td>1Ynm</td>
</tr>
<tr>
<td>2015</td>
<td></td>
<td></td>
<td></td>
<td>1Znm</td>
</tr>
<tr>
<td>2016</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Single-Module Steppers**
- Development Line
  - 300mm @ 2X nm

**Multi-Cluster Steppers**
- Production Ramp
  - >100wph @ 1X nm → 10 nm

**Technology Demos**
- 300mm & 450mm @ 26 nm → 10 nm

**Yield Targets & Production CoO**
- Prod. CoO, < 8nm O/L @ 26nm → 10nm

**Production Ramp**
- >100wph @ 1X nm → 10 nm
## Commercial Mask Supply

<table>
<thead>
<tr>
<th></th>
<th>Target</th>
<th>2012</th>
<th>X: 2.47nm, 3σ</th>
<th>Y: 2.23nm, 3σ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master/Replica @ 2x nm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master defectivity (cm⁻²)</td>
<td>0</td>
<td>0 with repair</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Replica added image placement (nm, 3σ)</td>
<td>&lt; 2</td>
<td>&lt;2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Replica defect density cm⁻²</td>
<td>&lt;1</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Replica CDU (nm, 3σ)</td>
<td>2</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Defect repair of masters</td>
<td>Yes</td>
<td>In use</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Image Placement

- **X: 2.47nm, 3σ**
- **Y: 2.23nm, 3σ**

---

### 6025 Imprint Mask

- TEM image 15nm HP

### Imprinted Resist Lines

- 15nm HP
Overlay Performance

Number of fields measured: 32
Number of points per field: 30

<table>
<thead>
<tr>
<th></th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw Mean</td>
<td>-0.10</td>
<td>-0.63</td>
</tr>
<tr>
<td>Raw 3sigma</td>
<td>9.40</td>
<td>9.68</td>
</tr>
<tr>
<td>Mean + 3sigma</td>
<td>9.5</td>
<td>10.31</td>
</tr>
</tbody>
</table>

- Biggest error sources:
  - Replica Imprint mask image placement
  - Wafer chuck anomalies

Further improvements to the mask and to the wafer chuck have resulted in current mix and etch overlay of **8nm**
Defectivity Improvements

Several orders of magnitude improvement over last two years

- Precise mask separation control
- Onboard resist filtration system

Low defect adders from imprint during multiple wafer runs

- 4.7 pcs/cm² per lot (25 wafers)
Toshiba presented during 2012 SEMATECH Litho Forum and stated verbally that yields >90% have been achieved at 10 meter line on a few runs.

Even more progress expected with next generation onboard resist filtration and mask replica defect improvements.
For High Volume Manufacturing, resist fill times of less than 1 second are required for stepper system throughput of > 100 wph (300 mm)

Keys to Fast Fluid Fill
- Small drop volume: Pico liter sized drops
- GDS based volume targeting
- Fluid front control
- Low viscosity imprint resists
- Materials optimized for wetting and filling performance
J-FIL Cost of Ownership Advantage

**TODAY**

- Optical Baseline
- Optical Double Spacer Patterning

**FUTURE**

- Optical Quad Spacer Patterning
- J-FIL Single Patterning

(M$^2$I Estimate)

---

**ASML Estimate**

---

**Step 1**
- Bottom mandrel ACL dep

**Step 2**
- Oxide dep

**Step 3**
- Top mandrel ACL dep

**Step 4**
- Nitride cap dep

**Step 5**
- BARC deposition

**Step 6**
- EUV litho

**Step 7**
- BARC etch

**Step 8**
- Nitride cap etch

**Step 9**
- Top mandrel ACL etch

**Step 10**
- Wet strip of nitride cap

**Step 11**
- Nitride spacer 1 dep

**Step 12**
- Nitride etch back

**Step 13**
- Top mandrel strip

**Step 14**
- Oxide strip

**Step 15**
- Bottom mandrel etch

**Step 16**
- Wet clean of & strip

**Step 17**
- Nitride spacer 2 dep

**Step 18**
- Nitride etch back

**Step 19**
- Bottom mandrel strip

**Step 20**
- Cut layer litho & process

**Step 21**
- Pad layer litho & process
Large semiconductor manufacturer has plans to ramp J-FIL™ into advanced memory production in 2014!

- Multiple systems already installed for nanoimprint performance refinement and device process integration

- Industry infrastructure readiness;
  - Equipment partner experienced in building and shipping J-FIL™ steppers
  - High quality DNP commercial imprints masks available today
Semiconductor Platform Roadmap

Equipment Partner
(Multi-Modules Stepper System)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Imprint Modules

- **IM20**
  - Development Line
  - Yield Targets @ 10nm

- **IM30**
  - Production
  - Prod. CoO, < 8nm O/L @ 26nm → 10nm

MII Systems

- **Imprio 300**
  - Technology Demo
  - 300mm @ 2X nm

- **Imprio 450**
  - Development Line & 450mm ETW
  - 300mm & 450mm @ 26 nm → 10 nm

Mask Replication

- 3Xnm
- 2Xnm
- 1Xnm
- 1Ynm → 10nm
Imprio™ 450
Advanced Lithography
Molecular Imprints Awarded Contract from Leading IC Manufacturer to Provide Lithography Equipment and Wafer Patterning Services in Support of the Semiconductor Industry’s 450mm Wafer Initiative

- PO Received Nov 2011
- Tool Accepted Dec 2012
- Wafer Services have begun Mar 2013

<table>
<thead>
<tr>
<th>Year</th>
<th>PO Received</th>
<th>Tool Build</th>
<th>450mm Wafer Services</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2014</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Intel is managing all 450mm patterned wafer inquiries
MII is the Only Company Producing 450mm Patterned Wafers Today!
“Litho cost has recently soared to ~50% of total wafer processing cost” *

Field-Scale Processing
- Optical Lithography*
- Nanoimprint Steppers
- Die-to-Die Inspection

Wafer-Scale Processing
- Etch
- Deposition
- CMP
- *Large Area Nanoimprint

* http://www.lithoguru.com/scientist/essays/why450.html
J-FIL is already being scaled for Hard Disk Drive (HDD) and Flat Panel Display large area substrates

- Throughput 65mm HDD platters runs at 700 disks per hour with a CoO of less than 50 cents per disk!

450mm Backend Patterning Could leverage the same CoO advantages

- Integrated resist jetting eliminates the need for track
- Resist jetting has zero waste for significantly reduced consumable cost
- Estimated 200+ WPH based on established models

Molecular Imprints has some early customer pull for 450mm Wafer Scale Backend Lithography and is currently qualifying opportunity
Summary

- Molecular Imprints systems continue to progress towards manufacturing ramp within the next 18 months
  - Defectivity, overlay, throughput performance within striking distance

- Industry infrastructure also preparing for 300mm ramp in 2014
  - Equipment partner’s cluster module stepper in development
  - DNP’s imprint mask capabilities achieving defectivity specs with impressive early 15nm 1X mask results

- Imprio 450 platform is ready today and under contract to provide patterning services to enable industry’s 450mm timeline
  - Intel is managing wafer demand inquiries
Acknowledgements