Litho Process Challenges in 20nm Logic Node and Wish List for Track Suppliers

Yayi Wei, Mark Kelling
Outline

- Lithographic technology requirements
- Major technical challenges at 20nm node
- Positive resist plus negative tone developer (solvent develop process)
- Special requirements for the solvent develop process
- Tighter coating control/bake temperature control
- Reduction of LWR and pattern-collapse
- Track productivity and COO
### Lithographic technology requirements

<table>
<thead>
<tr>
<th>Node (nm)</th>
<th>Contacted Poly Pitch (nm)</th>
<th>Metal Pitch (nm)</th>
<th>Minimum $k_1$</th>
<th>CDU (nm)</th>
<th>Critical Overlay (nm)</th>
<th>Block Level Overlay (nm)</th>
<th>Critical Layer Solutions</th>
<th>Ready for Test Chip</th>
<th>HVM Start</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>100</td>
<td>80</td>
<td>0.28</td>
<td>2.0</td>
<td>6</td>
<td>12</td>
<td>Immersion + double exposure</td>
<td>2010</td>
<td>2012</td>
</tr>
<tr>
<td>20</td>
<td>86</td>
<td>64</td>
<td>0.22*</td>
<td>1.8</td>
<td>4-5</td>
<td>12</td>
<td>Immersion + (Pitch Split) + DFM</td>
<td>2011</td>
<td>2013</td>
</tr>
</tbody>
</table>

- **Overlay**
  - Requirements include contributions from reticles, process and metrology, as well as exposure tool.
  - Overlay ≤ 8 nm and beyond will require tool dedication.
  - If pitch splitting is used for 20 nm, overlay of 4-5nm will be required.

- **CD control (ACLV)**
  - Requirement includes reticles, OPC, resist processing and LER.
  - CDU numbers are post-etch on product ($3\sigma$)
Technical challenges at 20nm node

- Aggressive SMO scheme - Programmable illumination and computational lithography
- Advanced tool control that was first introduced at 32nm needs to be further improved:
  - Exact control of the overlay baseline, including non-linear wafer and field terms
  - Generic tool control and matching is mandatory
  - Non-linear corrections at product in case where wafer distortions need to be corrected
- Overlay performance required to meet design rules and process assumptions
  - Immersion tool to block level tool matching improvement
  - Implement higher order wafer alignment (HOWA) terms (3rd or 5th order) for special cases where we have wafer distortions, like DT.
- Non-destructive metrology solution
  - 193i resist is very sensitive to e-beam and current CD-SEM causes resist shrinkage
  - New metrology solution is being investigated/implemented, such as scatterometry
- Defect inspection and control strategies
- Tight CDU control
- **Interruptive technology solution – Solvent develop process**
• Litho stack
  - OPL 100nm
  - SiARC 35nm
  - Resist 105nm (NTD resist vs. PTD resist)
• Anchor
  - P128nm/L50nm for NTD
  - P128nm/S50nm for PTD
• Target CD: S36nm ± 10%
• NA: 1.35
• Dipole 90X/ Ypol / Sigma 0.5/0.7

<table>
<thead>
<tr>
<th></th>
<th>EL max (%)</th>
<th>DOF@5% (µm)</th>
<th>MEEF</th>
<th>LER (nm)@BDBF</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTD</td>
<td>17.7</td>
<td>0.135</td>
<td>1.9</td>
<td>3.2</td>
</tr>
<tr>
<td>PTD</td>
<td>11</td>
<td>0.120</td>
<td>2.4</td>
<td>5.3</td>
</tr>
</tbody>
</table>

• It offers better litho PW for small trench and at tip-to-tip.
What the solvent develop process can do for 20nm critical levels?

- Metal level has a pitch of 64 nm
  - Double patterning (LELE) is the solution prior to the availability of EUV.
  - The solvent develop process provides the litho solution for small trenches (P128nmS32nm).

- Metal levels with 64 nm pitch require vias with a minimum pitch of 64nm × 1.41 ≈ 90nm.
  - The solvent develop process can provide better aerial image
  - Single exposure plus solvent develop process is the primary solution
Special requirements for the solvent process

- **Material aspect - Mainly in develop module**
  - Developer is a solvent, NOT aqueous TMAH.
  - Rinse liquid is another solvent, NOT DI water.
    - 4-methyl-2-pentanol

- **Process aspect**
  - Adhesion
    - Resist line collapse on SiARC
  - Delay effect
    - Trench CD shrinkage of 1-2nm/h during development delay (q-time)
  - Develop module
    - Developer flow rate has minimal influence on CD, CDU or CDU profile (Dynamic developer dispense)
    - Puddle process improves CDU and CDU profile
20nm node requires a resist thickness of 90-100nm in critical layers. The thickness variation must be controlled in $3\sigma \leq 1$ nm.

- Defects in spin-coated resist film $\leq 0.01/cm^2$
- Defects in wafer backside $\leq 0.28/cm^2$
- PEB bake temperature sensitivity spec for 193i resist is $1.5nm/^\circ C$.
- 20nm node requires CDU=1.8nm ($3\sigma$). Hot plate must have the temperature uniformity $\sim 0.5^\circ C$ across 12” wafer.
Reduction of LWR and pattern-collapse

- LWR (3σ) must be smaller than 8% of CD, i.e. ~2.6nm for 20nm critical layers.
- Pattern collapse is a serious issue in advanced nodes. Surfactanated developer and surfactant rinse are still the effective way to enhance the line-collapse margin. Innovative solutions for line-collapse in solvent develop process are needed.
- Optimization of developer nozzle and dispense method for hydrophobic resists
Track productivity and COO

- Reducing scheduled/un-scheduled down time
  - Foundry business requires lower break-even capacity load
  - High throughput and small down time are appreciated.

- Resist consumption
  - Spin-coating has the tendency of wasting materials for good uniformity
  - Any innovative solution to use photoresist more efficiently is welcome (193i resist is very expensive – several k$/gal)
Thank you!

Trademark Attribution

GLOBALFOUNDRIES, the GLOBALFOUNDRIES logo and combinations thereof are trademarks of GLOBALFOUNDRIES Inc. in the United States and/or other jurisdictions. Other names used in this presentation are for identification purposes only and may be trademarks of their respective owners.