“Shooting for the 22nm Lithography Goal” with the SOKUDO DUO Coat/Develop Track
Three (3) different exposure options for 22nm:

- MAPPER Lithography on E-Beam Maskless (ML2)
- ASML on EUV Lithography & M.P. Immersion ArF
- NIKON on Multiple Patterning Immersion ArF & EUVL

One (1) in-line coat/develop track fits all scenarios:
However, coat/develop track configuration varies significantly by photolithography technology ...

Throughput (wph) Projections

<table>
<thead>
<tr>
<th></th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
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</thead>
<tbody>
<tr>
<td>E-Beam</td>
<td>1 – 5</td>
<td>5 – 10</td>
<td>60 – 100*</td>
<td>100+*</td>
<td>120+*</td>
</tr>
<tr>
<td>EUV</td>
<td>30 – 60</td>
<td>60 – 100</td>
<td>80 – 125</td>
<td>125+</td>
<td>150+</td>
</tr>
</tbody>
</table>

wph = wafers per hour
* Assumes E-Beam (ML2) Cluster Tool such as MAPPER Litho.

Resist Process Steps on Track

<table>
<thead>
<tr>
<th>UL / Barc Coat</th>
<th>Resist Coat</th>
<th>Top Coat</th>
<th>Backside Clean</th>
<th>Bevel Clean</th>
<th>Post E. Rinse</th>
<th>Develop</th>
</tr>
</thead>
<tbody>
<tr>
<td>E-Beam</td>
<td>■</td>
<td>■</td>
<td>-</td>
<td>■</td>
<td>-</td>
<td>■</td>
</tr>
<tr>
<td>EUV</td>
<td>■</td>
<td>■</td>
<td>-</td>
<td>■</td>
<td>-</td>
<td>■</td>
</tr>
<tr>
<td>Immersion</td>
<td>■</td>
<td>■</td>
<td>▲ ▲</td>
<td>■</td>
<td>■</td>
<td>■</td>
</tr>
</tbody>
</table>
SOKUDO Coat/Develop Track 22nm Process Development

- **imec** Double Patterning LPLE
  - Materials & Process Benchmarking 32nm → 26nm

- **SELETE** EUV Lithography Resist Qual.
  - New resist process evaluations @ SELETE

- **CEA LETI** E-Beam DW Qualification
  - MAPPER Lithography E-Beam Process R&D
Immiscion Lithography with SOKUDO

- Immersion Resist Process Defectivity: Microbridging & Resist Filtration
- CoO Study for Double Patterning Lithography
- CDU optimization for immersion lithography & Double Patterning:
  - JSR’s litho-freeze-litho process (freeze coat, thermal freeze)
  - TOK’s posi-posi process “Freeze-Free”
“Photo” Double Patterning Resist Process on Track

<table>
<thead>
<tr>
<th></th>
<th>Freeze Coat chemical b/w 1st &amp; 2nd Resist</th>
<th>Self-Freeze by 2nd Resist Coat &amp; Bake</th>
<th>Thermal freeze bake</th>
</tr>
</thead>
<tbody>
<tr>
<td>JSR</td>
<td><img src="kar%C5%9F%C4%B1la%C5%9Ft%C4%B1" alt="Smiley" /></td>
<td><img src="kar%C5%9F%C4%B1la%C5%9Ft%C4%B1" alt="Smiley" /></td>
<td><img src="kar%C5%9F%C4%B1la%C5%9Ft%C4%B1" alt="Smiley" /></td>
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<tr>
<td>TOK</td>
<td><img src="kar%C5%9F%C4%B1la%C5%9Ft%C4%B1" alt="Smiley" /></td>
<td><img src="kar%C5%9F%C4%B1la%C5%9Ft%C4%B1" alt="Smiley" /></td>
<td><img src="kar%C5%9F%C4%B1la%C5%9Ft%C4%B1" alt="Smiley" /></td>
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<tr>
<td>Dow Elec. Mtrl.</td>
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<tr>
<td>Shin-Etsu</td>
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<td>Sumitomo</td>
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**EXP** – **CP** – **PAB** – **SC(Resist 1)** – **CP** – **PAB** – **SC(BARC)** – **CP** – **AHP**

START

**Litho 1**

**PEB** – **CP** – **DEV (+)** – **HB** – **CP** –

**Litho 2**

**EXP** – **CP** – **PAB** – **SC(Resist 2)** – **CP** –

**COAT**

**DEVELOP**

**PEB** – **CP** – **DEV (+)** – **HB** – **CP** –

END
JSR Freeze Coat & Thermal Freeze Comparison
32nm Feature Target CD-SEM Images

Freeze Coat

Litho 1 @ L1

Litho 1 @ L2

Combined L1:L2 Pattern

Thermal Freeze

Litho Coat

CD Growth

CD Shrink
JSR Thermal-Freeze 26nm L/S Target CDU

The CD uniformity data with the thermal freeze process comparable to traditional litho-etch-litho-etch and spacer double patterning CDU.

Layer 1

- Mean: 27.00nm
- CDU 3σ: 1.85nm

Layer 2

- Mean: 26.75nm
- CDU 3σ: 1.35nm

Substrate: ARC®29-SR (105nm)
Layer 1: Non-TC thermal freeze resist (FT=60nm, 130C/125C, SCA/RCA/ACA=90°/76°/94°)
Layer 2: Non-TC normal resist (FT=50nm, 100C/95C, SCA/RCA/ACA=92°/80°/95°)
Exposure: 39nmL96nmP with att-PSM, NA=1.35, Dipole40X, 0.747/0.626, Y-Polarization
Development: ECO Nozzle(OPD262/DIW)
integration for ASML NXE:3100 (EUV)

- SOKUDO EUVL Coat/Develop Track Configurations ~120wph
  - Coat: Underlayer, Resist
  - Develop: TMAH / TBAH developers; various rinse approaches
  - Bake: Biased Hot Plate (QBH) for CDU control / tuning;
    “Q” Quick set-temperature change bake between lots
Maximize EUV Lithocell Utilization:
Exposure Test Lot Run + R&D Eval. Wafers **simultaneously**

---

**ASML NXE:3100**

Pilot Test Lot Run

R&D Eval. Wafers

---

Always keep critical EUV scanner running when available!
KEY for R&D + Pilot Line Productivity!
E-Beam Experience by SOKUDO

- **Advantest F-100 (Japan)**
  - SOKUDO RF3 Coat, Developer in-line with E-Beam

- **Vistec SB3054DW @ leti Grenoble (France)**
  - SOKUDO RF3 off-line for E-Beam
    - in-line with Nikon NSR-S307

45nm Double Patterning Process

- 1st litho
  - PR
  - BARC
  - 1st PR printing

- 1st etch
  - PR
  - BARC open
  - 1st PR stripping

- 2nd litho
  - PR
  - BARC deposition

- 2nd etch
  - PR
  - BARC open
  - 2nd PR stripping
The End Goal...

E-Beam Coat/Develop Track in-line with MAPPER

MAPPER E-Beam Cluster
Target 100 WPH

SOKUDO DUO Track
~100-120 WPH

2C = Underlayer
2C = RESIST
4D = DEVELOP
+ Backside Scrub
+ E-Beam interface
EUV, E-Beam Common Resist Process Development Focus Points

- Resist Manufacturers Continuously Reformulating for
  - Line Width Roughness (LWR)
  - Sensitivity to Dose
  - Resolution 32 nm → 22 nm

- 32 nm → 22 nm CD LWR, Pattern Collapse & Defectivity
  Track Process Studies:
  - Develop methods, solutions
  - Rinse methods, solutions

Reference: SPIE 7636-27, February 2010, San Jose, CA USA

Material approach

LWR < 1.7 nm

Out-gassing TBD

Trade-off

Sensitivity < 10 mJ/cm²

Resolution < 52 nm

ITRS Roadmap for 52 nm node EUV resists

Reference: SPIE 7636-27, February 2010, San Jose, CA USA
## SOKUDO EUVL Technical Papers History

### SPIE Advanced Lithography 2009

<table>
<thead>
<tr>
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<td>Development of EUV resists at Selete</td>
<td>SELETE (SOKUDO assignee, Koji Kaneyama)</td>
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<tr>
<td>7273-115</td>
<td>EUV resist processing in vacuum</td>
<td>SELETE, SOKUDO</td>
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### International Symposium on EUVL 2009

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<td>Resist II</td>
<td>EUV resist materials and processing at Selete</td>
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<td>Poster 94</td>
<td>Study of post-develop defect on typical EUV resist</td>
<td>SOKUDO</td>
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<td>7636-115</td>
<td>Alternative resist processes for LWR reduction in EUVL</td>
<td>SELETE (SOKUDO assignee, Koji Kaneyama)</td>
</tr>
<tr>
<td>7639-26</td>
<td>Development of EUV-resists based on various new materials</td>
<td>SELETE (SOKUDO assignee, Koji Kaneyama)</td>
</tr>
<tr>
<td>7636-27</td>
<td>Development of resist material process for hp 2x nm devices using EUV lithography</td>
<td>SELETE (SOKUDO assignee, Koji Kaneyama)</td>
</tr>
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Coat, Bake & Develop Track Process Knobs for EUV / E-Beam resist development

**SPIN COAT**
- Dispense Chemistries:
  - Underlayer +
  - Photo Resist
- Thin-film coating recipe
  - 40-60nm thickness

**BAKE & CHILL**
- Post-Expose (PEB) for CD Uniformity control
- High Temp. (PAB, BARC)

**DEVELOP**
- Defect Control Approach
  - Wafer Rinse & Dry
  - Surfactant Rinse
- Developer Chemistries:
  - TMAH, TBAH(?)
  - Negative Develop(?)
**PEB in vacuum vs. atmosphere**

**Summary:**
Results depend on resist; PEB in vacuum may be low value-added.

**Table 3. The lithographic performance of MET-2D with PEB in vacuum and atmosphere**

<table>
<thead>
<tr>
<th>Item</th>
<th>in Vacuum</th>
<th>in Atmosphere</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top-view SEM Image @45nmL/S (1:1)</td>
<td>[Image]</td>
<td>[Image]</td>
</tr>
<tr>
<td>Cross-section SEM Image</td>
<td>[Image]</td>
<td>[Image]</td>
</tr>
<tr>
<td>Esiz@45nmL/S [mJ/cm²]</td>
<td>14.1</td>
<td>13.7</td>
</tr>
<tr>
<td>Resolution limit [nm]</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>LWR [nm]</td>
<td>6.1</td>
<td>&gt; 7.8</td>
</tr>
</tbody>
</table>

**Table 4. The lithographic performance of SSR3 with PEB in vacuum and atmosphere**

<table>
<thead>
<tr>
<th>Item</th>
<th>in Vacuum</th>
<th>in Atmosphere</th>
</tr>
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<tbody>
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<tr>
<td>Cross-section SEM Image</td>
<td>[Image]</td>
<td>[Image]</td>
</tr>
<tr>
<td>Esiz@45nmL/S [mJ/cm²]</td>
<td>16.0</td>
<td>&gt; 11.2</td>
</tr>
<tr>
<td>Resolution limit [nm]</td>
<td>30</td>
<td>&gt; 25</td>
</tr>
<tr>
<td>LWR [nm]</td>
<td>6.2</td>
<td>&gt; 4.9</td>
</tr>
</tbody>
</table>

**Reference:** EUV resist processing in vacuum, Koji Kaneyama, Shinji Kobayashi, Toshiro Itani; Proc. SPIE 7273-115 (2009)
TBAH Developer extends CD capability, reduces pattern collapse

Reference: EUV resist materials and processing at Selete, K. Matsunaga, et.al., International Symposium on EUV Lithography, October 2009, Prague
Pattern Collapse limiting EUV resist resolution

Sensitivity – Resolution

Model of pattern collapse and improvement by process

Tensile stress

Surface tension

Stress

\[ \sigma = \frac{6 \gamma \cos \theta}{d} \left( \frac{H}{L} \right)^2 \]

H. Namatsu, Appl. Phys. Lett. 66 (20), 1995

- Thinner resist thickness
- Rinse solution
- Additional under layer

Swelling

- Developer concentration
- Developer with surfactant
- Bulky developer solution

Condition: SFET NA0.3, Illum. Annular (0.7/0.3), Thick: 60nm

Reference: SPIE 7636-27, February 2010, San Jose, CA USA
EUV resists improving with each new generation: Resolution, LWR, Sensitivity

**Sensitivity – Resolution**

- **Pattern collapse**
- **SSR4**
- **SSR2**
- **SSR4+Process**

**Sensitivity - LWR**

- **SSR2**
- **SSR3**
- **SSR4+Process**
- **SSR4**

**E_{size} of hp32nm (mJ/cm^2)**

**E_{size} of hp32nm (mJ/cm^2)**

Reference: SPIE 7636-27, February 2010, San Jose, CA USA

Selete

32nm Targets: Sensitivity ($E_{size}$) : 10mJ/cm^2
Short-range LWR : $hp \times 10\%$
Common / specific defect history; EUV study started

- **MUV**: $\lambda \geq 365\text{nm}$
- **KrF**: $\lambda = 248\text{nm}$
- **ArF**: $\lambda = 193\text{nm}$
- **ArF immersion**
- **EUV**: $\lambda = 13.5\text{nm}$

**Common Defects**
- **Blob**
- **Residue**

**Specific Defects**
- **micro-Bubble**
- **Bottom-ARC**
- **$\mu$-Bridge**
- **Water Droplet before PEB**
- **None**
EUV & E-Beam ...

- Although EUV may be leading the march towards 22 nm, E-Beam can close gap with (MAPPER) throughput plans for improvement towards 2012+

- SOKUDO participating in EUV and E-Beam collaborations
  - EUVL consortia resist evaluations and characterization
  - E-Beam IMAGINE project resist process qualification

- EUV and E-Beam resists following similar trends and challenges:
  - In parallel transitioning from 32nm → 22 nm process development
  - Both resist systems largely based on reformulating i/KrF generation blends
  - Resist trending to thinner coatings: 40-60 nm target thickness
  - Resolution – LWR – Sensitivity (RLS) all common issues
“Shooting for the 22nm Lithography Goal” with the SOKUDO DUO Coat/Develop Track