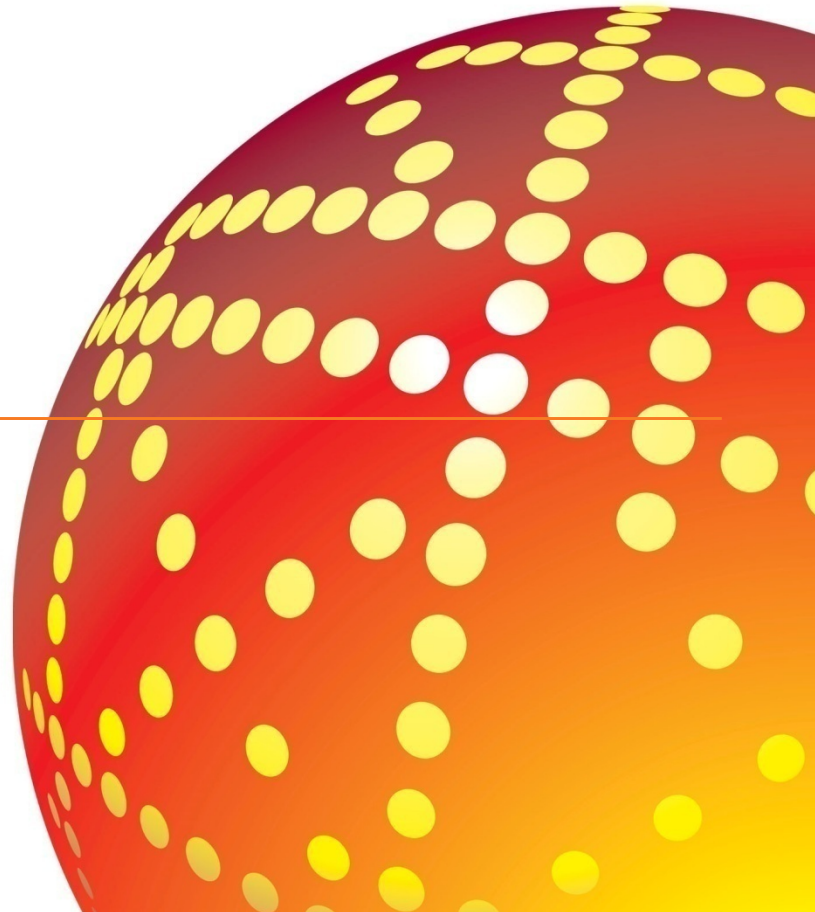
Logic Double Patterning at Pitches Below 80 nm

Sokudo Lithography Forum
Semicon West 2009

Tom Wallow

GLOBALFOUNDRIES



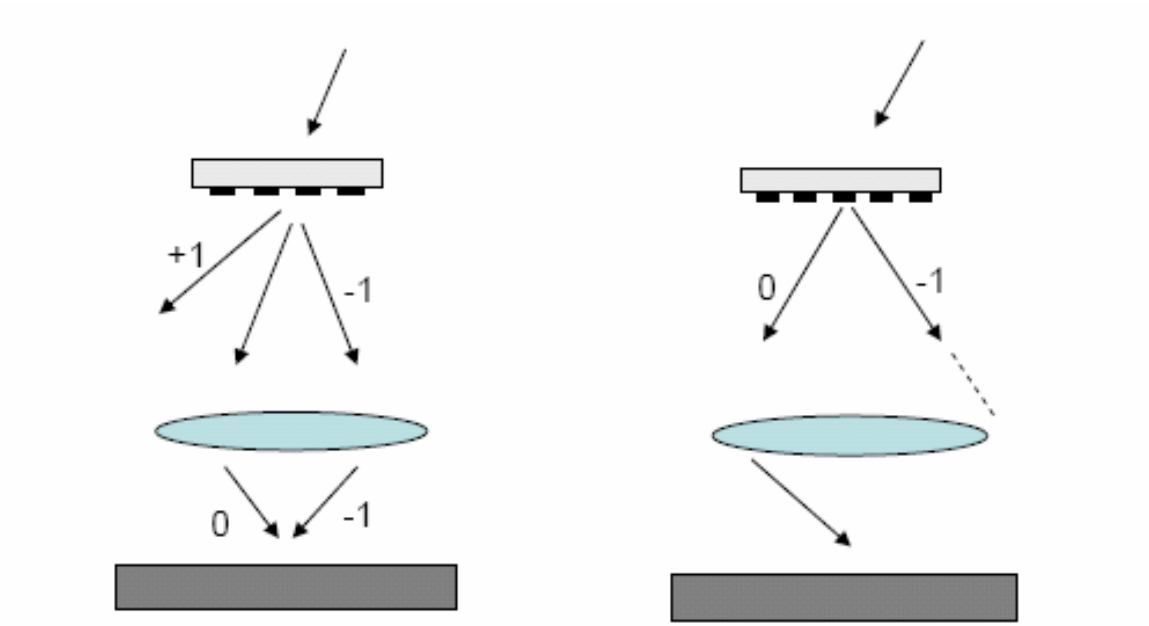
Logic Pathfinding Complexity Below 80 nm

- Lithography challenges
  - too many to mention
- Design challenges
  - living with simpler geometries
- Process challenges
  - cost-effective double patterning
- Materials challenges
  - for resists, size matters as much as wavelength

- → Why does all this matter for tracks?

The Low-k_1 Lithographic Resolution Regime

Low k_1: $0.5 > k_1 >$ $k_1 <$



Only 2 diffracted orders form image at wafer plane

Only 1 diffracted order captured
No modulation at wafer plane

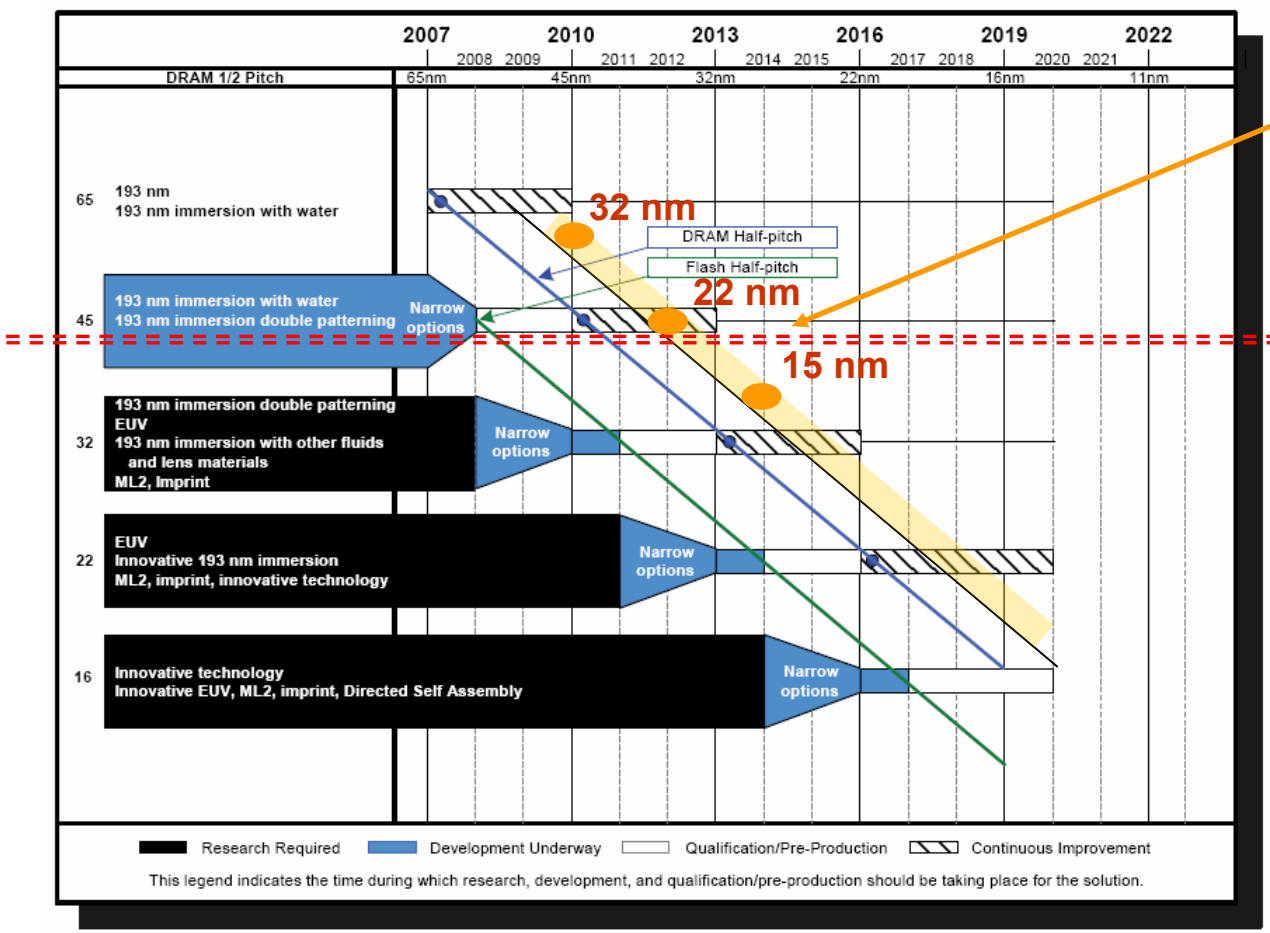
$$\frac{p}{2} = k_1 \frac{\lambda}{NA}$$

$NA_{(max)} = 1.35$

$k_{1(min)} \sim 0.28$

→ $p_{(min)} \sim 80$ nm

ITRS Lithography Roadmap 2007

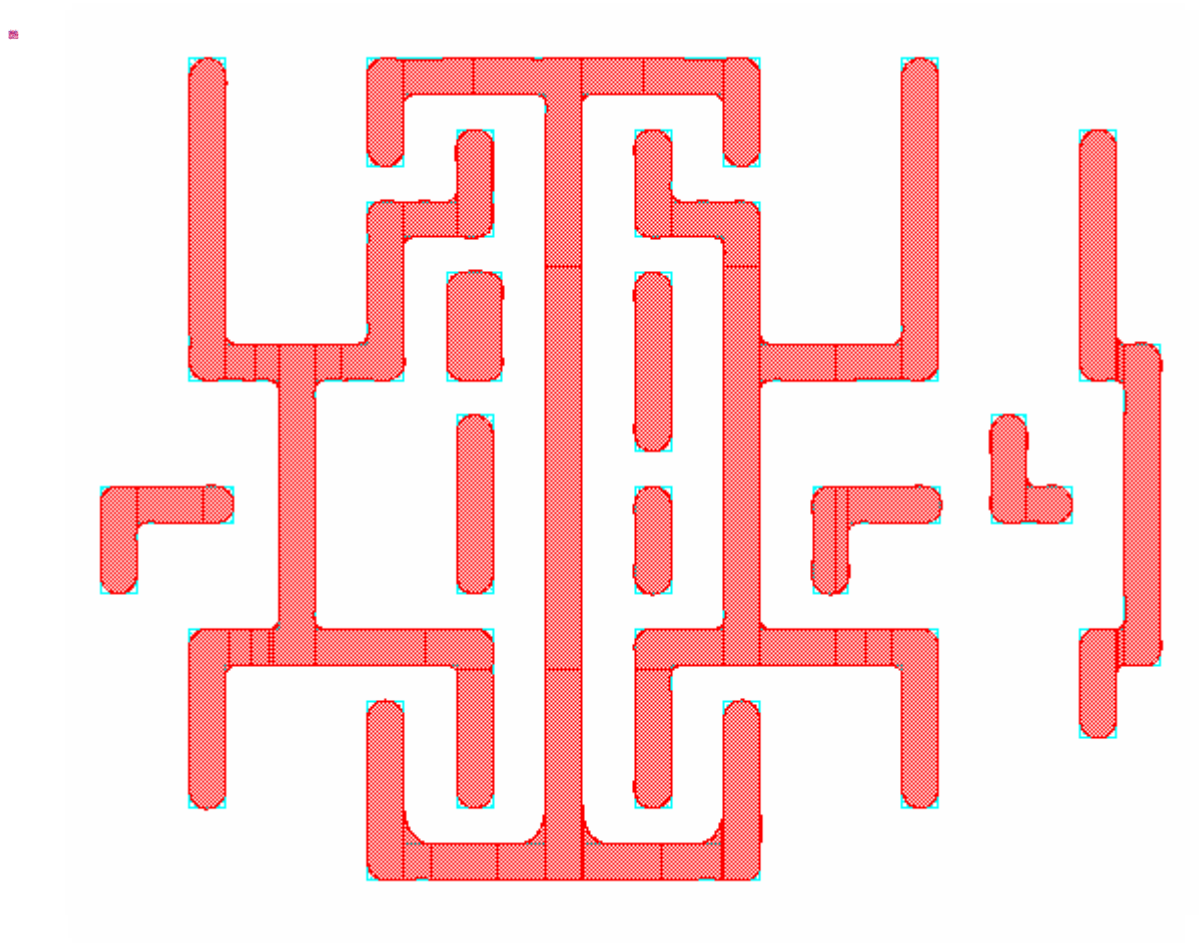


Logic nodes

80 nm pitch

- Logic pitch is relaxed vs. DRAM, but will transition below 80 nm for 15 nm node.

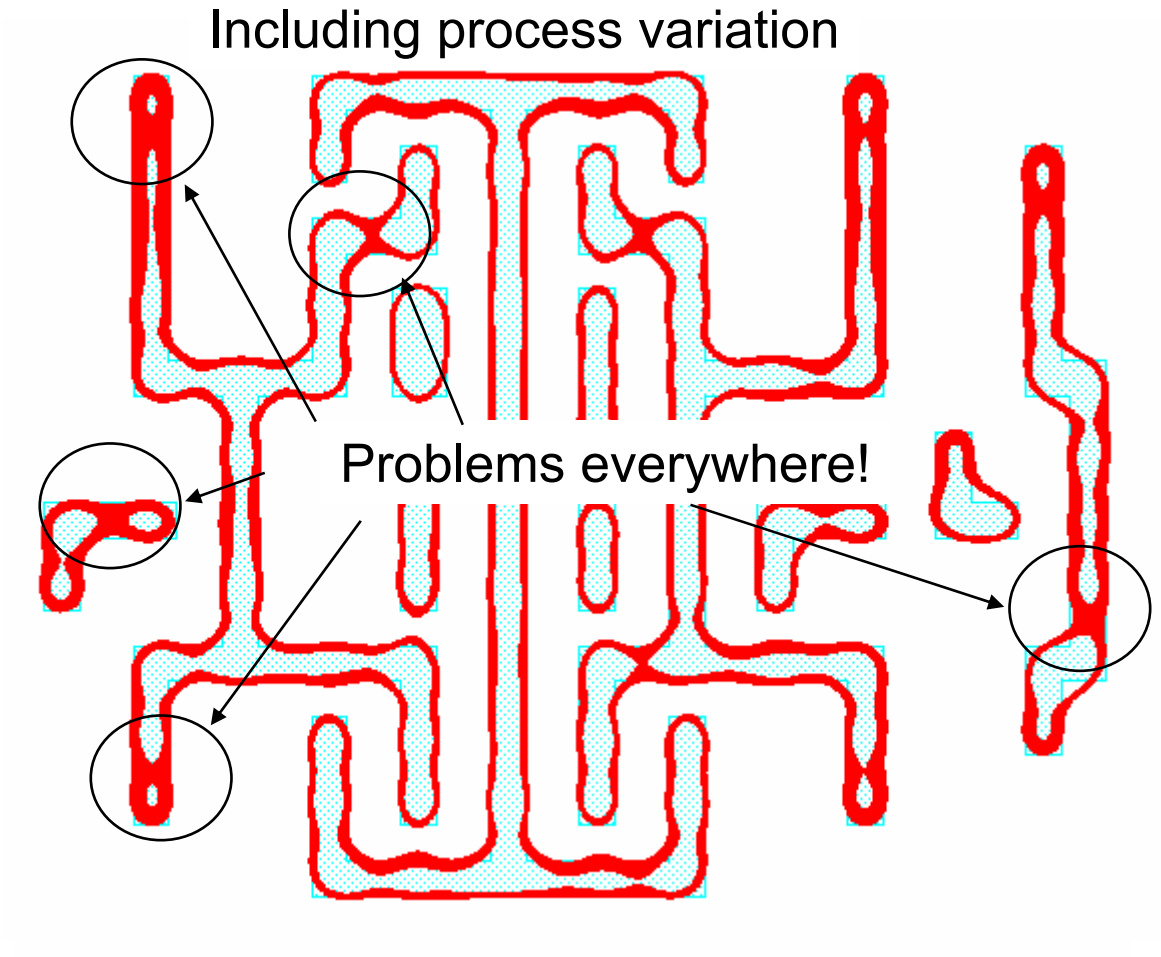
Patterning and k_1 Factor



Process Improvement RB OPC

$k_1 > 0.6$

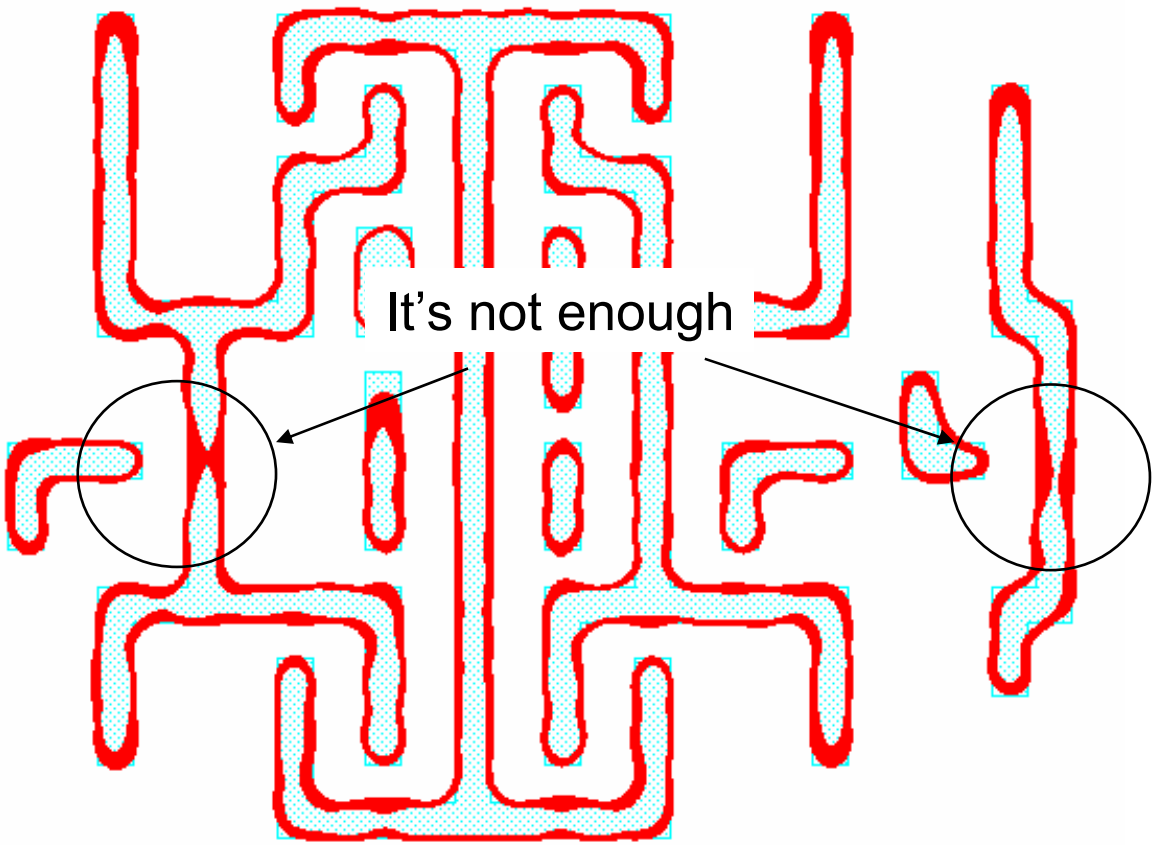
Patterning and k_1 Factor



Process Improvement RB OPC

$k_1 \rightarrow 0.35$

Patterning and k_1 Factor

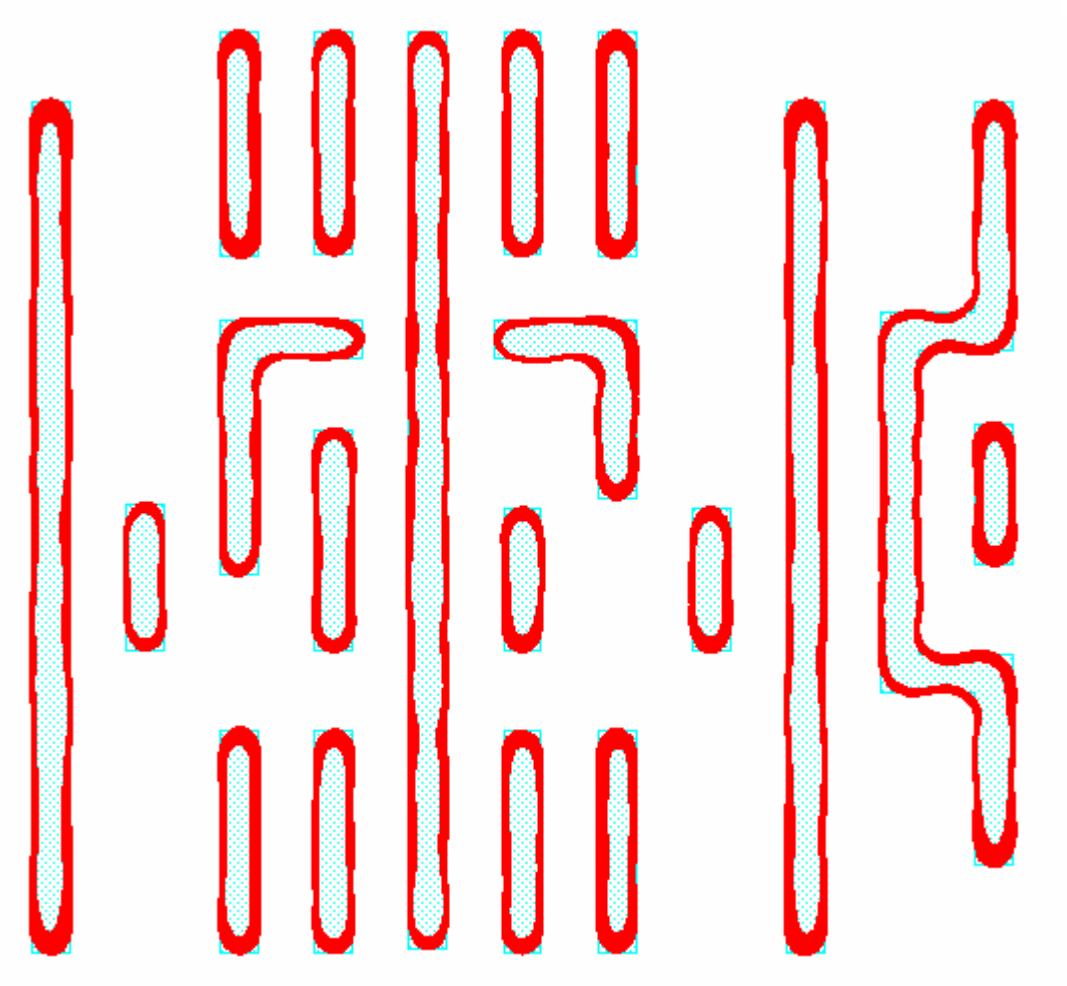


k_1 ~ 0.35

Process Improvement RB OPC

MB OPC OAI

Patterning and k_1 Factor



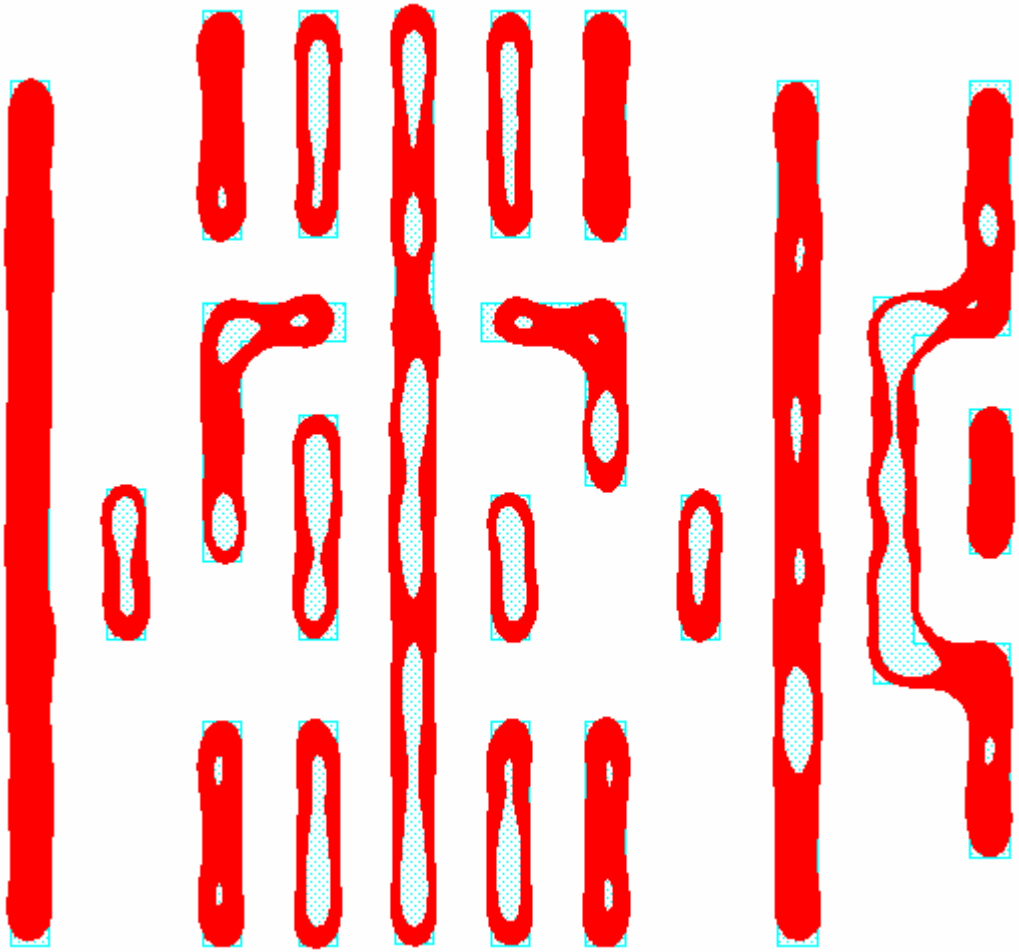
$k_1 = 0.35$

Process Improvement
RB OPC

MB OPC
OAI

RDR
DFM

Patterning and k_1 Factor



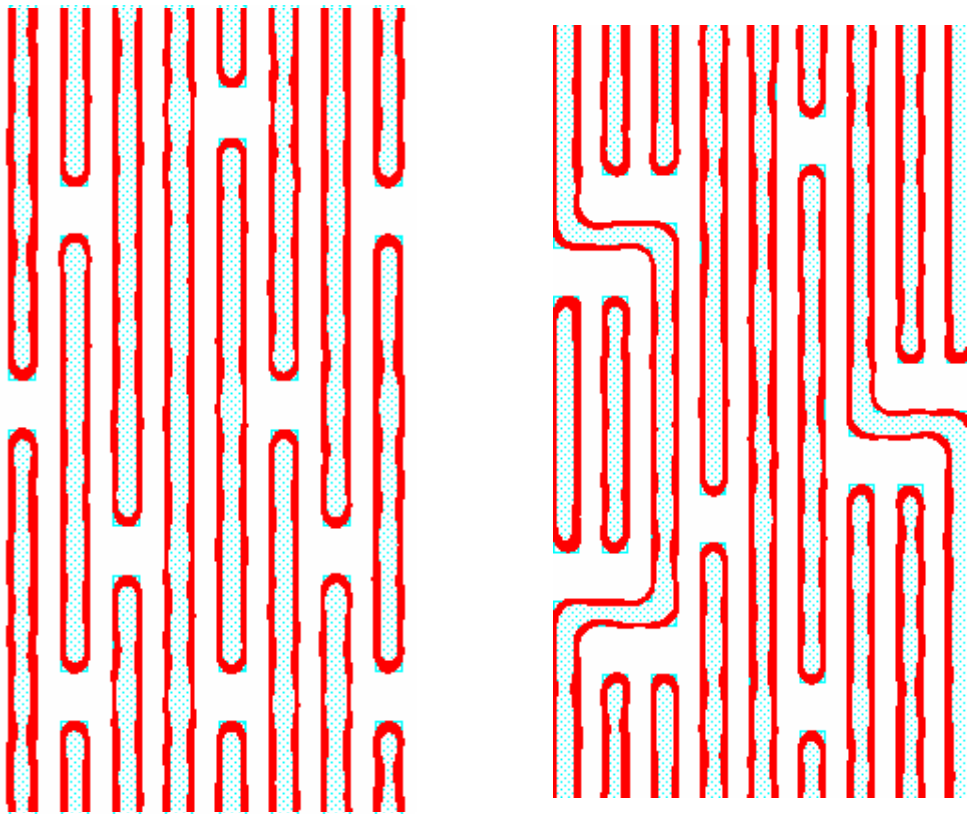
Process Improvement
RB OPC

MB OPC
OAI

RDR
DFM

k_1 ~ 0.3

Patterning and k_1 Factor



$k_1 \sim 0.28$

Process Improvement
RB OPC

MB OPC
OAI

RDR
DFM

DDL (DE)
Single Orientation
Cut Masks (LELE)

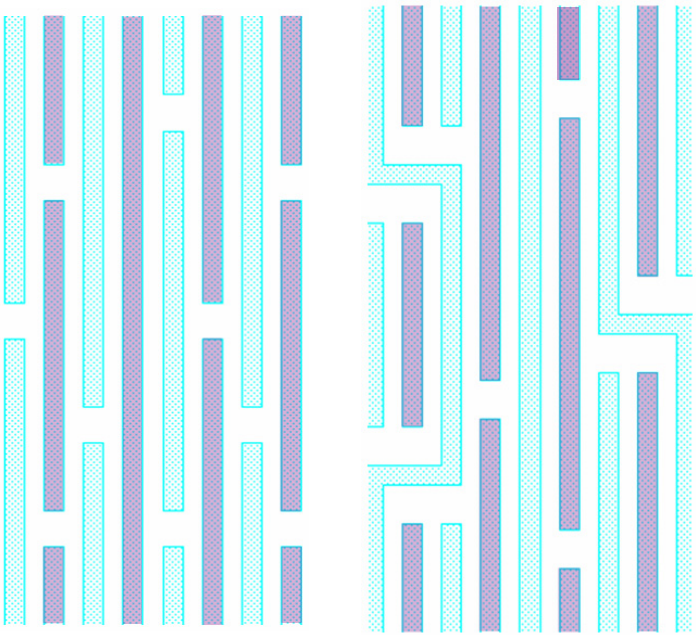
Transition at 80 nm Pitch for Logic

- 80 nm pitch is ultra-low k_1 factor
  - Unidirectional control only
  - Requires double patterning already, but not necessarily pitch-split
- Solutions at 80 nm must address:
  - Both 1D at 2D layout
  - Both brightfield and darkfield
  - (pitch splitting is not fundamentally required for 193i)
- Solutions below 80 nm must address:
  - Same issues as >80 nm, but with minimal increased mask count
  - (pitch splitting is fundamentally required for 193i)
- → Solutions for device and gate will not be same as solutions for contacts, metals, and vias

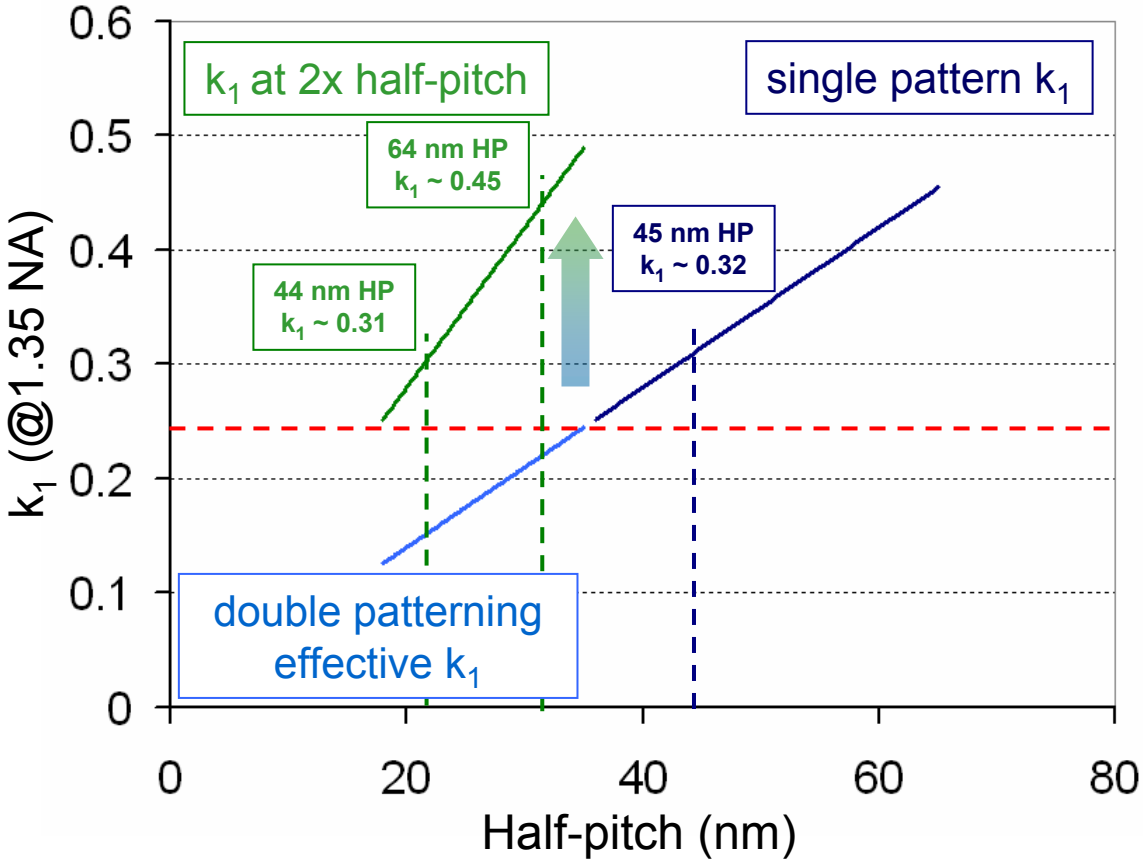
Options Below 80 nm

- Option 1: Pitch split double patterning
  - Litho-Etch-Litho-Etch (LELE)
  - Spacer patterning (SADP)
  - Litho-Freeze-Litho-Etch (LFLE)
- Option 2: EUV
- Option 3: Next generation lithography
  - NIL
  - DW EB
  - New technologies

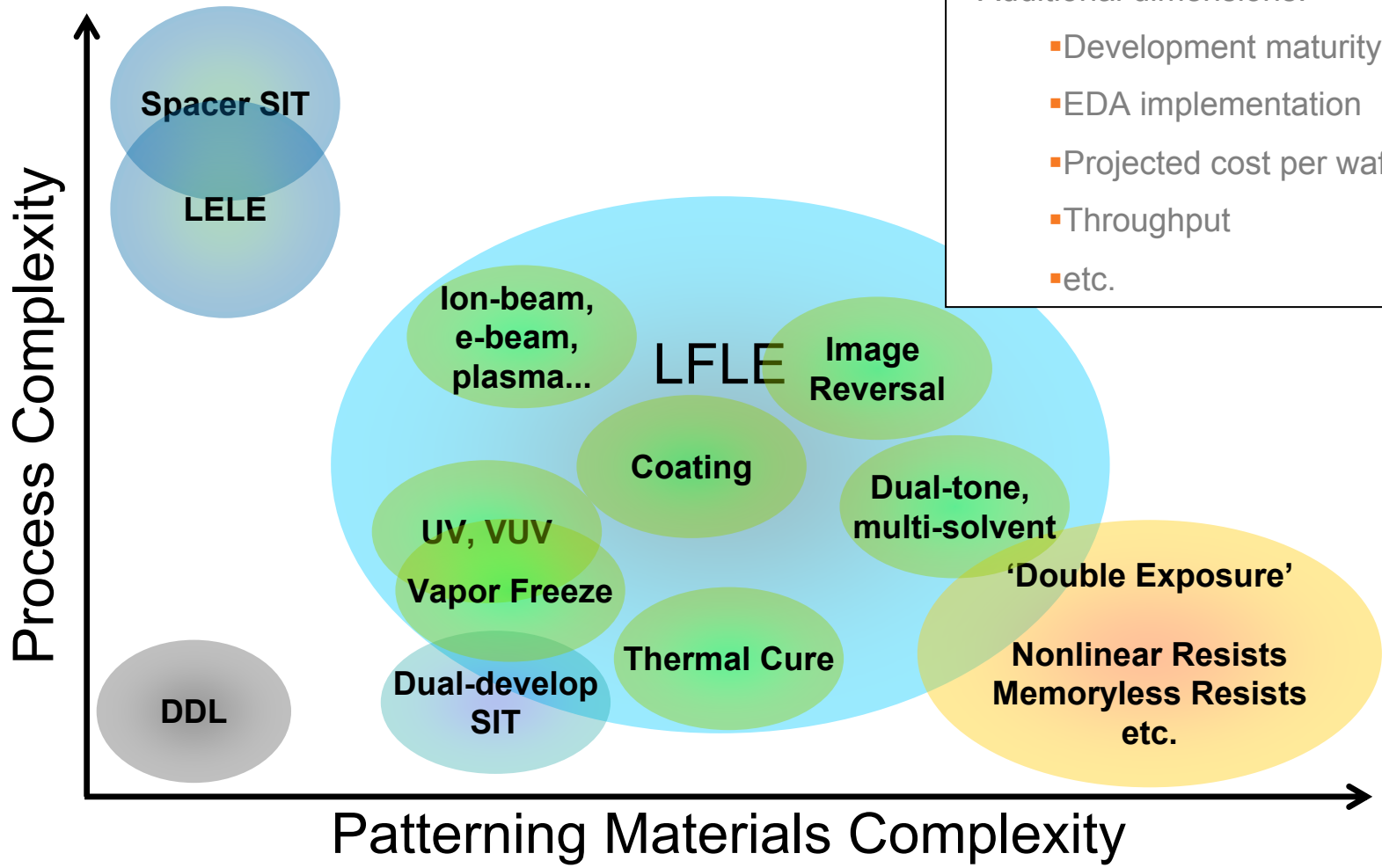
Effective k_1 Below 0.25: Pitch Splitting



- 32 nm HP k_1(effective) ~0.224
- 64 nm HP k_1 ~0.45



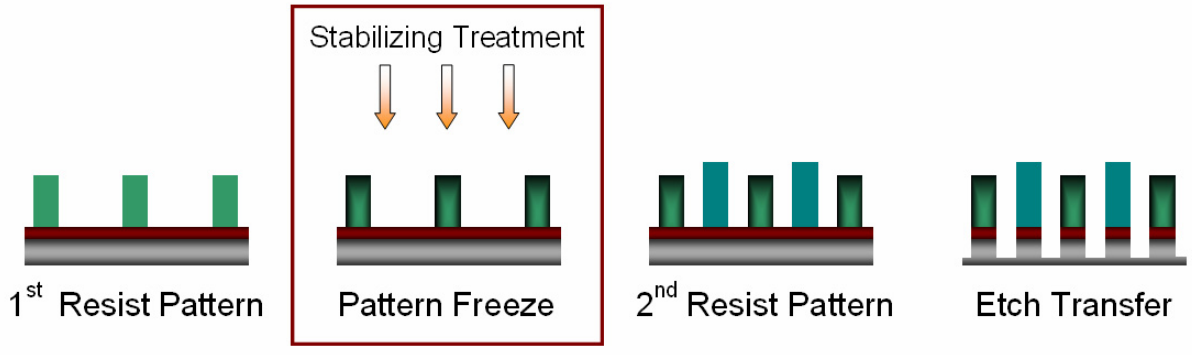
Double Patterning Options



- Additional dimensions:
  - Development maturity
  - EDA implementation
  - Projected cost per wafer level
  - Throughput
  - etc.

- Many process options are under development

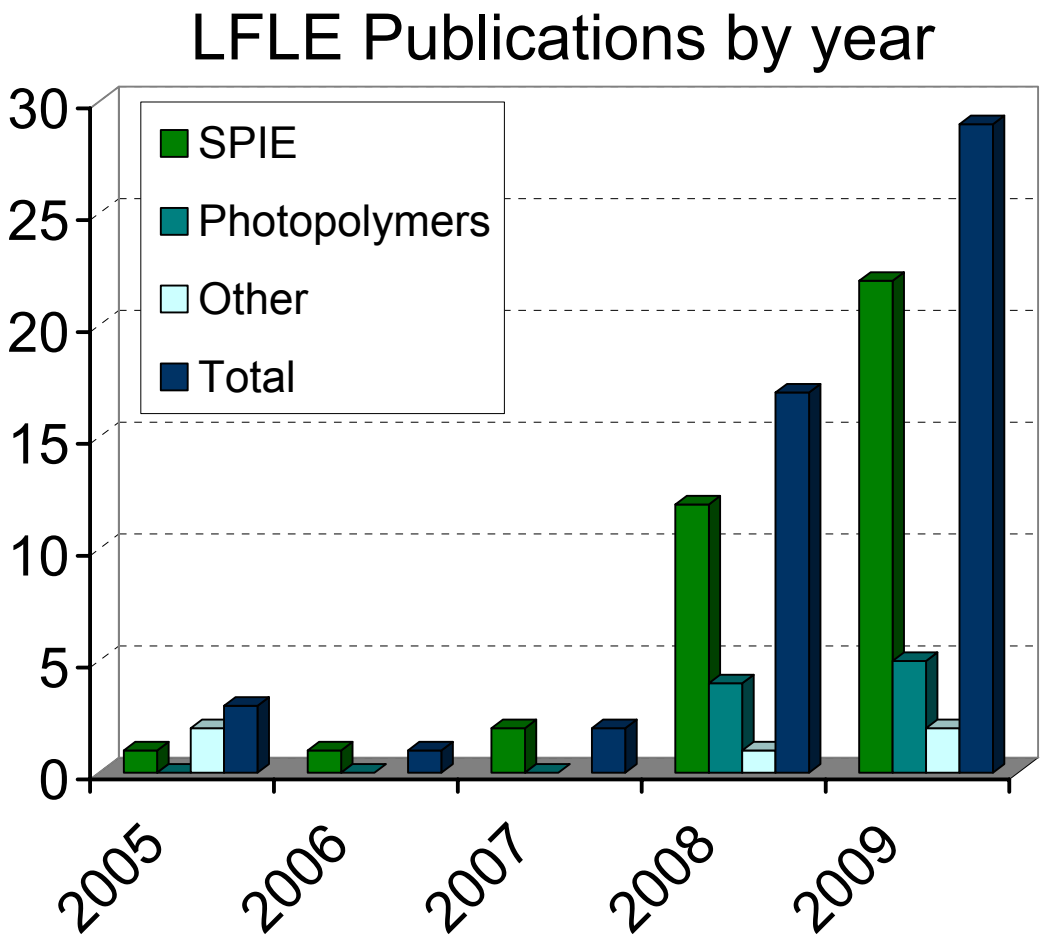
LFLE Processes



Thermal Cure | **Coating** | **Dual-tone, multi-solvent** | **Image Reversal** | **UV, VUV** | **Vapor Freeze** | **Ion-beam, e-beam, plasma...**

- Many outstanding materials and process innovations
- (Too many examples to include in .pdf version)

LFLE Interest



- Engagement by:
  - All resist suppliers
  - Major tool suppliers
  - Consortia
  - Semi Manufacturer R&D
  - EDA vendors

Steps Toward LFLE Maturity and Production Use

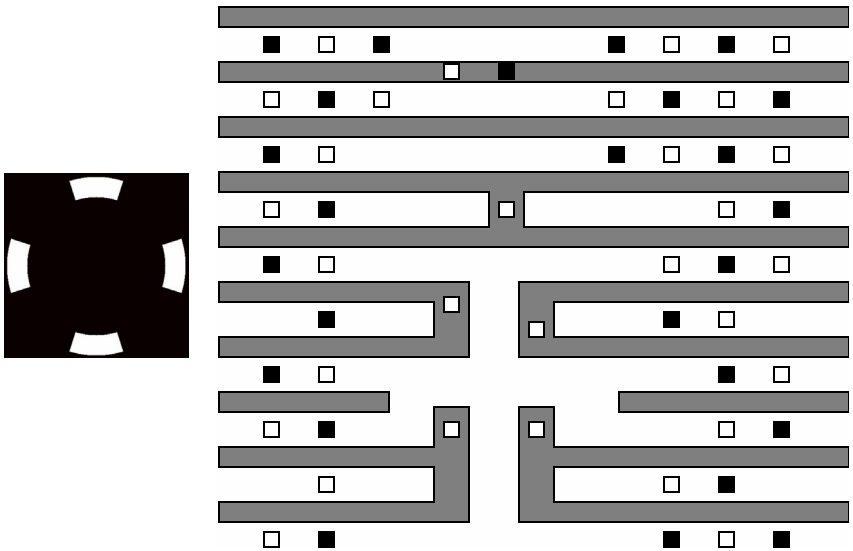
- Clear level targets for LFLE implementation
  - FEOL vs. BEOL
- Decomposition-friendly design; mature EDA tools
- Superior process and device performance
  - Minimal CDU contributions from additional LFLE process steps
  - Competitive defectivity and yield
- Throughput advantages
- Cost advantages

Where Does LFLE Fit?

- Brightfield: relatively straightforward examples
  - Gate level patterning with LFLE vs. incumbent methods
- Darkfield examples:
  - contacts
  - BEOL- trenches and vias
- → Fundamentally different implementations
- 'Decomposition-friendly' design

Examples of Contact/Via Double Patterning

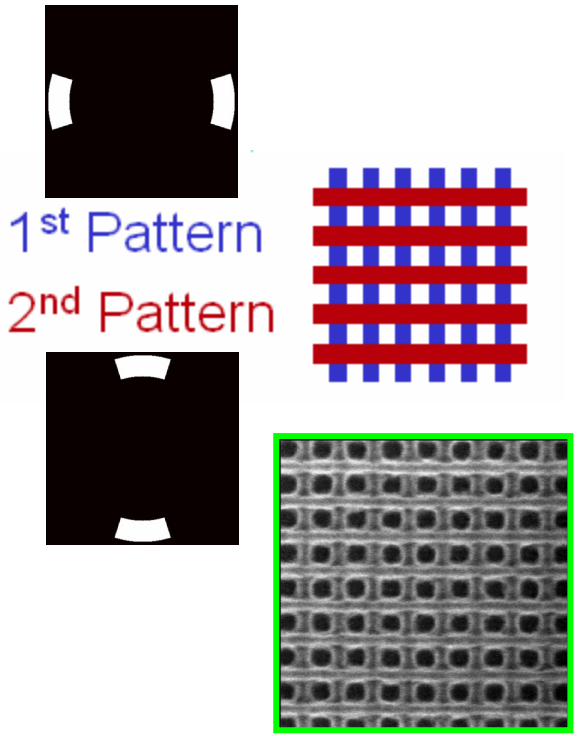
Checkerboard LELE



$k_1(\text{contacts}) = \sqrt{2} * k_1(\text{lines})$

-Burkhardt and Colburn, JVSTB 2009 (in press)

Cross-Grid LFLE

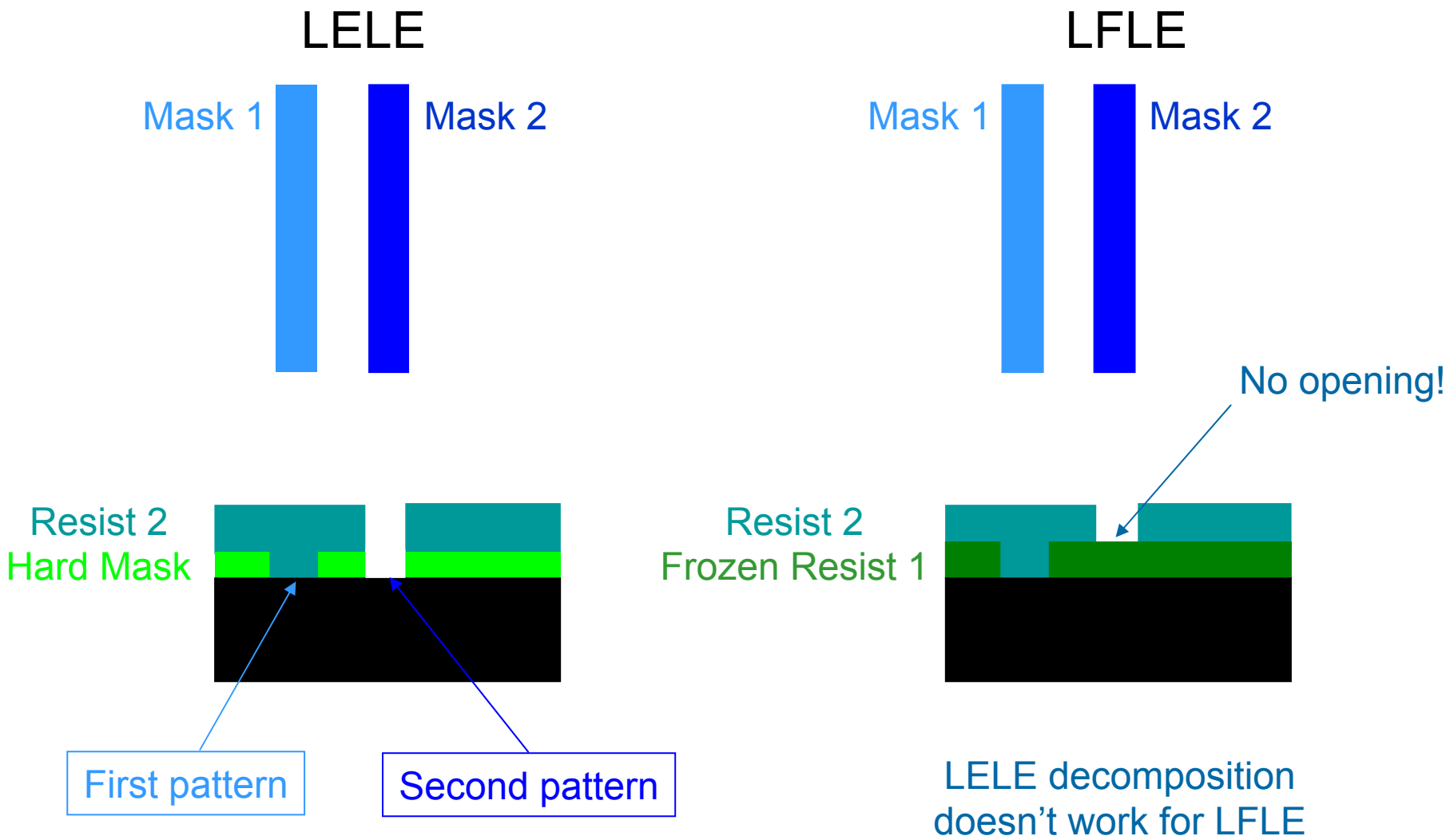


$k_1 \sim 0.28$

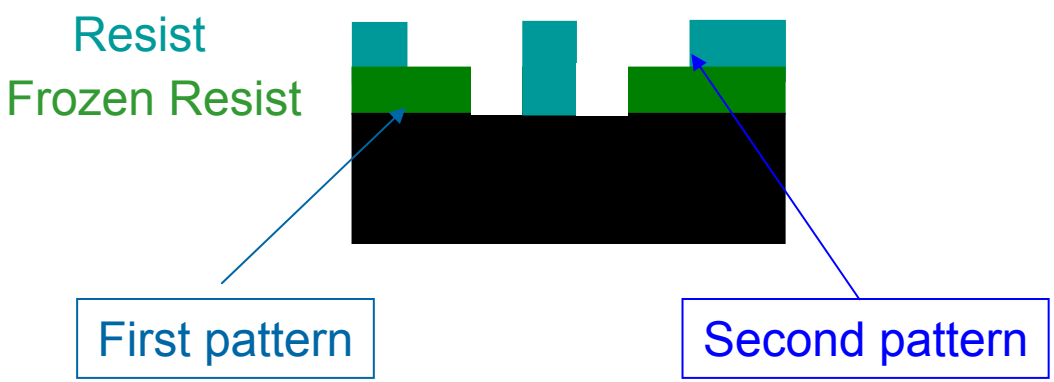
-many reports starting 2005

- Decomposition-friendly design is key
- How will these accommodate gate pitch <80nm?

LFLE Trench Pitch Splitting

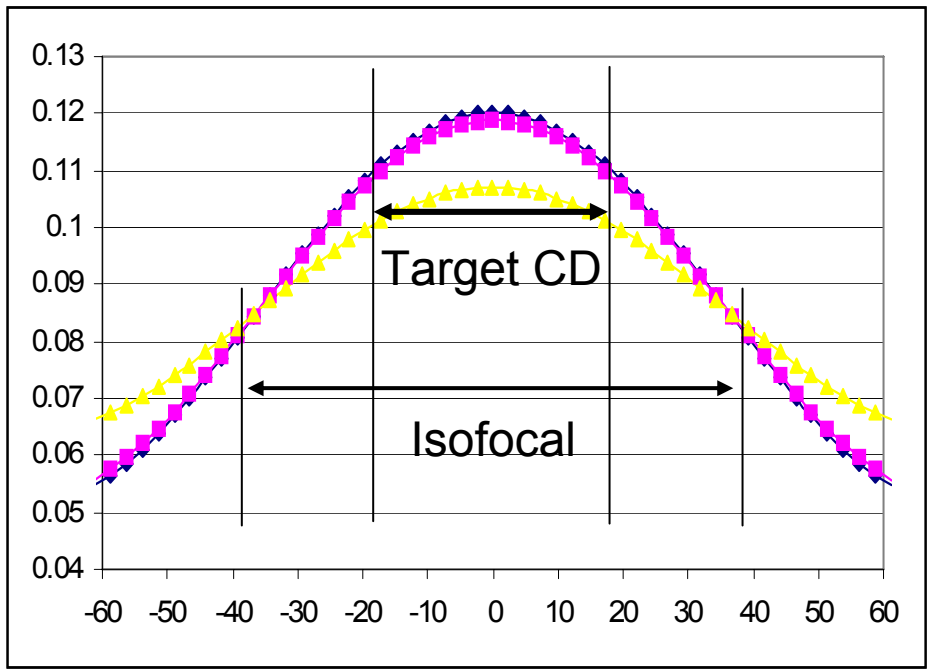


LFLE Trench Decomposition



What else may we need from Tracks for Double Patterning?

- Patterning at 1:3 duty cycle is harder...
  - Lines: Is trim etch enough?
  - Trenches and contacts: is taper etch enough?
  - Ancillaries
    - Track based vs. etch based
    - Cost of ownership

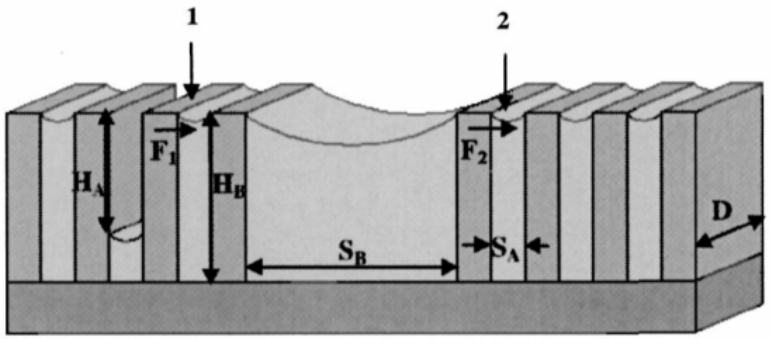


- → Additional modules, additional reagents, additional process steps

Other Resist Performance Limits Below 80 nm

- Fundamental materials properties scaling in ultrathin films
  - Materials strength scaling- pattern collapse
  - Resist structure homogeneity
    - component segregation
    - interfacial confinement
- Why discuss this in the context of track processing?
  - Resists become ‘stacks’
  - Ancillary processing gains in importance
  - More process steps, more coats, more reagents

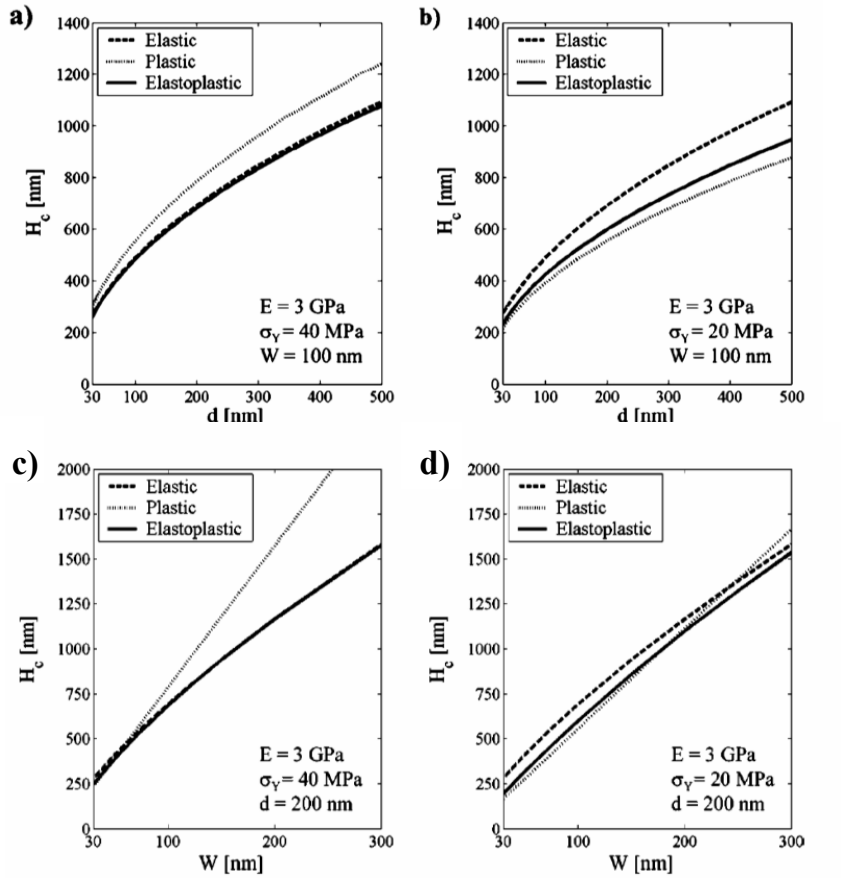
Pattern Collapse



$$F_1 = \text{Pressure} * \Delta Area = \left(\frac{2\gamma\cos\theta}{S_A}\right) * H_A D$$

$$F_2 = \Delta\,\text{Pressure} * Area = 2\gamma\cos\theta\left(\frac{1}{S_A} - \frac{1}{S_B}\right) * H_B D$$

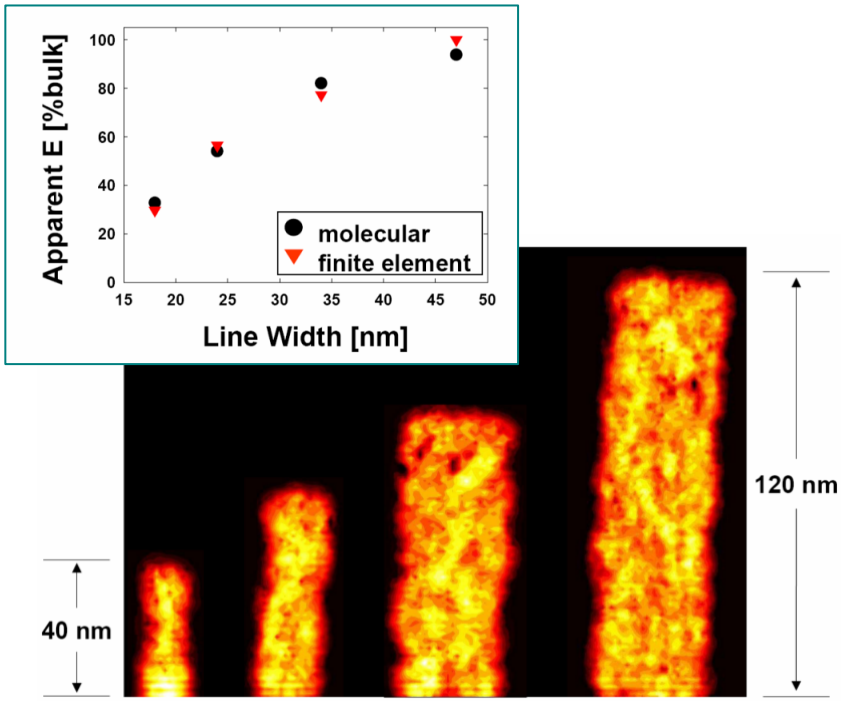
-Cao et al., JVSTB 2000



-Yoshimoto et al. J. Appl. Phys. 2004

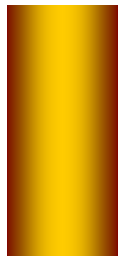
- Critical height for collapse (H_c) does not scale with CD for any current model
- Deviation from linear scaling becomes more severe as modulus decreases

Scaling of Materials Properties

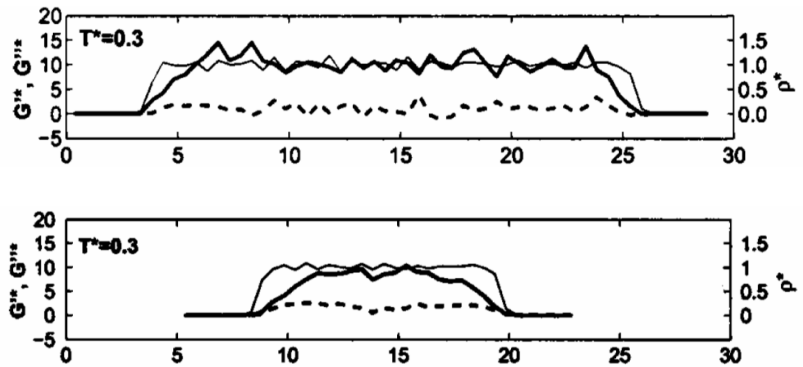


-Van Workum and de Pablo
Phys. Rev. Lett. 2003

Independent simulation methods predict nonlinear modulus decrease below 40 nm CD



Glassy core;
softened exterior

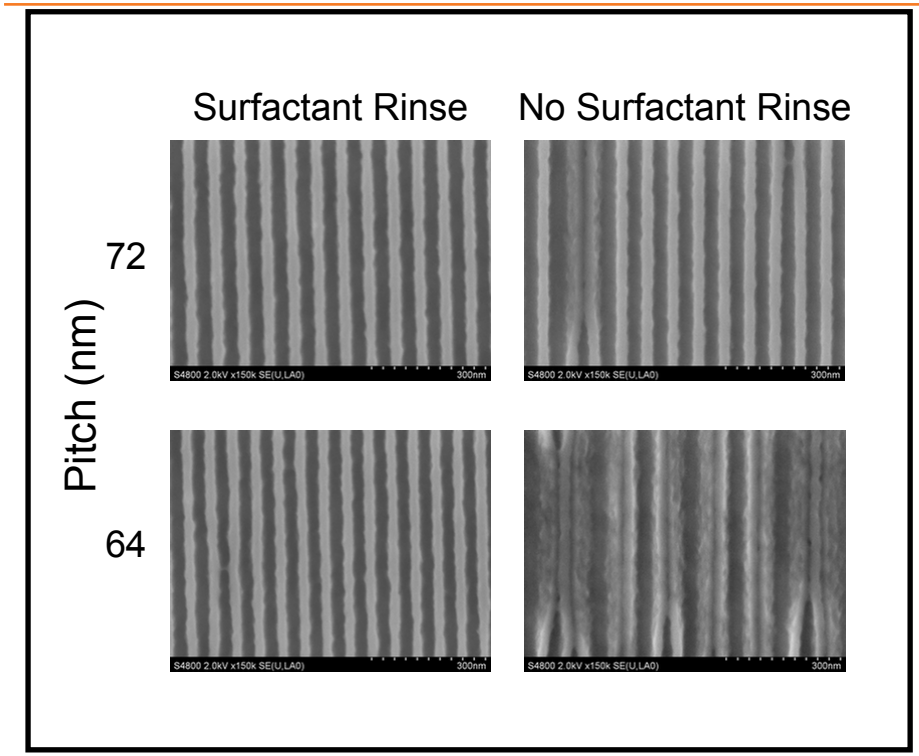


σ (MD segment size; σ ~1.5 nm)

-Yoshimoto et al.
J. Chem. Phys. 2005

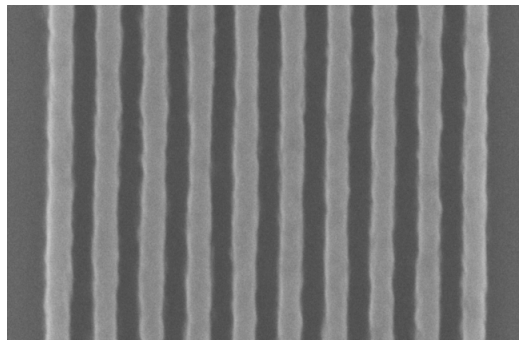
Softened shell grows vs. glassy core below 40 nm CD

Process Improvement with Development Modifications

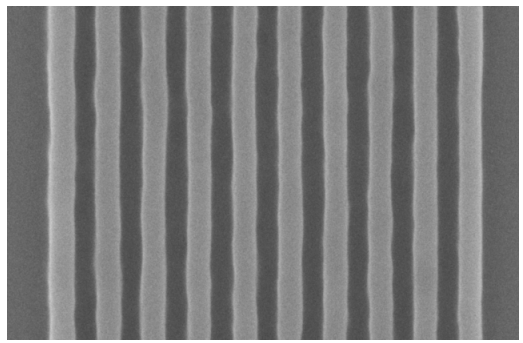


Pattern Collapse Suppression

-Sugiyama, M. et. al., Proc. SPIE 2007
-Jouve, A. et al., Proc. SPIE 2006
-Wallow, T. et al, Proc. SPIE 2008



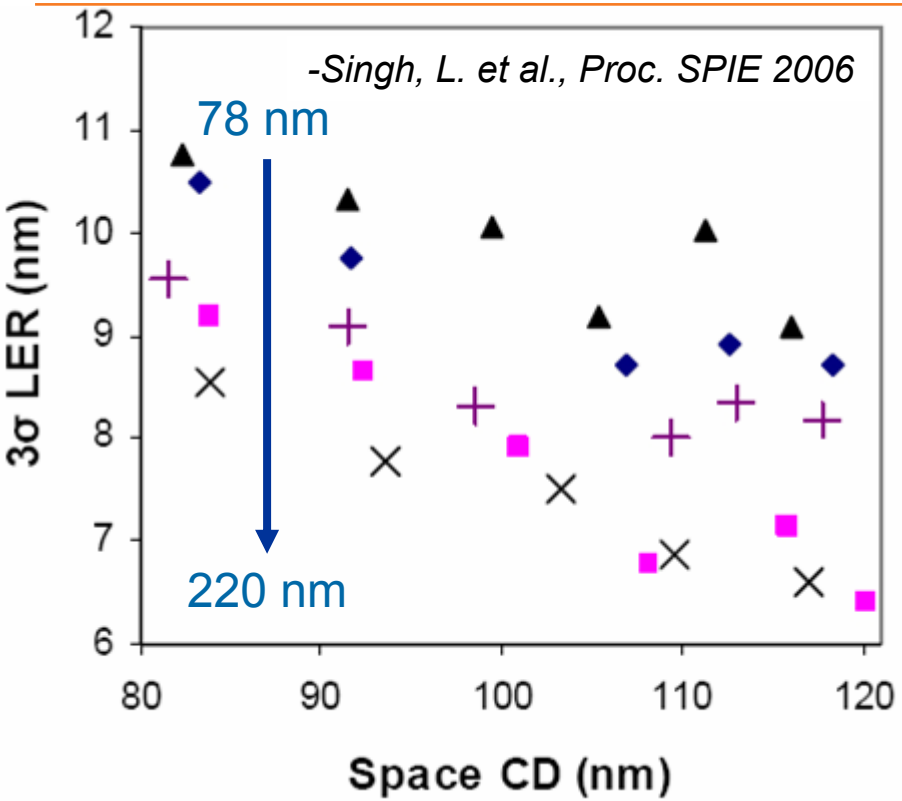
Baseline Process
LER = 4.3 +/- 0.4 nm

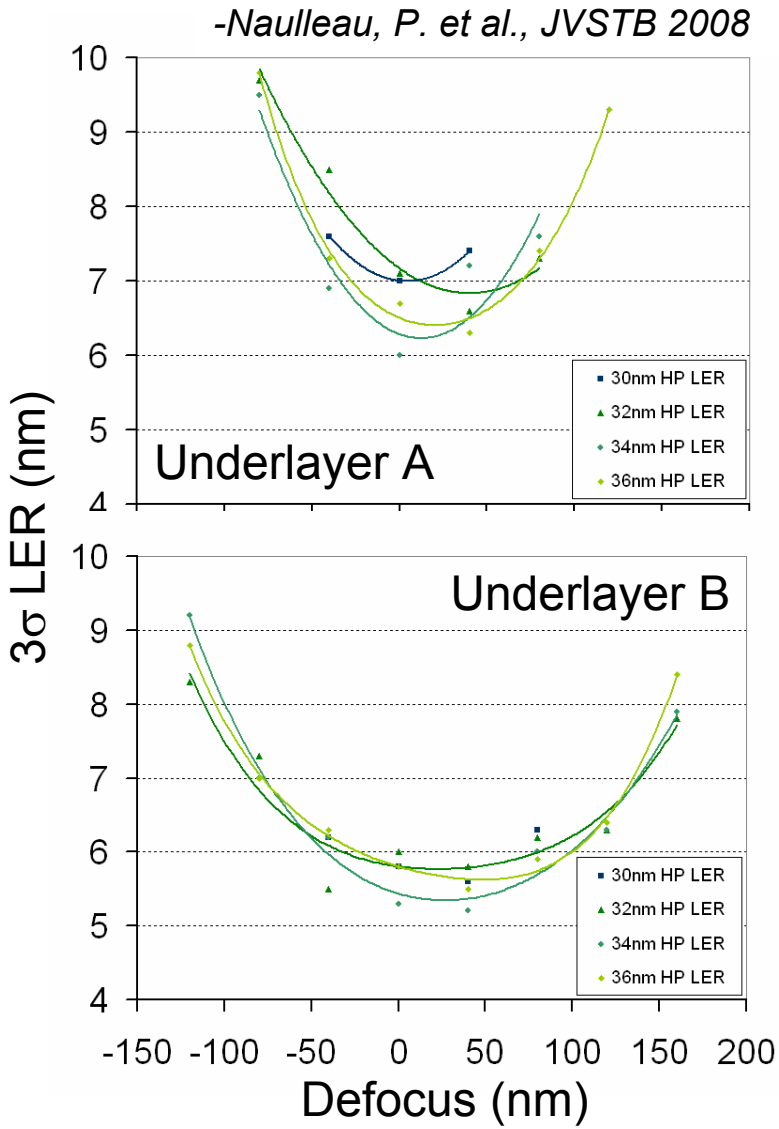


Surface Conditioner Process
LER = 3.2 +/- 0.4 nm

LER Reduction

Substrate Confinement Effects





- Reflectivity control is no longer enough
- Interfacial engineering
- Resist/interface matching- resist becomes a ‘stack’

Conclusions

- Regardless of which lithographic technologies win below 80 nm pitch, patterning processes will become more complex.
  - Double patterning: LFLE will require greater track flexibility and configurability vs. LELE
  - Double patterning: any method is likely to require more complex process flows to compensate for 1:3 duty cycle
  - Fundamental scaling: resist structures will be smaller, weaker, and more sensitive to stack and process. 'Nice to have' ancillary track processes are likely to become a necessity

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