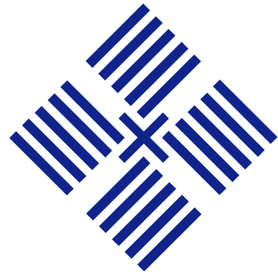


Holistic View of Lithography for Double Patterning

Skip Miller
ASML

Outline

- Lithography Requirements
- ASML Holistic Lithography Solutions
- Conclusions

Shrink Continues…Lithography keeps adding value

Average of multiple customers' input

Logic / SRAM

Logic

DRAM

NAND Flash

NAND

Unit Ce

Resolution/half pitch, "Shrink" [nm]

200
100
80
60
50
40
30
20

1/1/02 1/1/03 1/1/04 1/1/05 1/1/06 1/1/07 1/1/08 1/1/09 1/1/10 1/1/11 1/1/12 1/1/13 1/1/14 1/1/15

Year of production start*

6 Transistor SRAM Cell

k_1 0.40 ~ 0.44

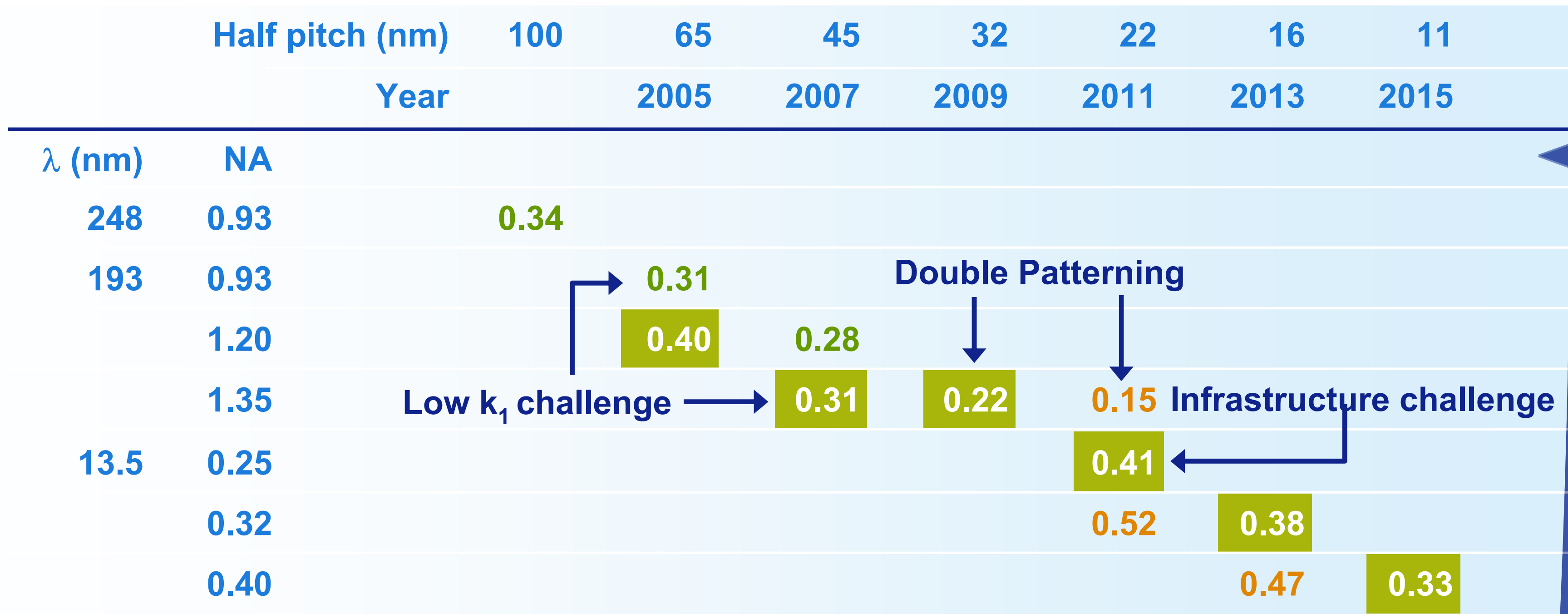
k_1 0.30 ~ 0.35

k_1 0.27 ~ 0.30

* Note: Process development 1.5 ~ 2 years in advance

Most Likely Lithography Roadmap

DPT will bridge gap between single exposure 193nm & EUV



k1 = (half-pitch) * numerical aperture / wavelength

Most likely
Opportunity
Unlikely

ASML

Options to print below immersion single exposure limit

Cost, complexity and cycle time

K1 > 0.25

K1 < 0.25

*Wafer does not leave the exposure system between the two exposures

*Wafer preferably does not leave the litho cell between the exposures

*Wafer leaves litho cell for etch between the exposures

- SiON /HM Etch
- Clean
- Strip
- Film Etch
- Metrology
- Develop
- Expose
- Top coat
- Resist
- BARC
- SiON / SiC
- Hard Mask
- Device film
- Si

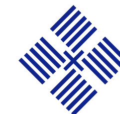
Single exposure

Double exposure

Litho DPT - LFLE

Litho DPT - LELE

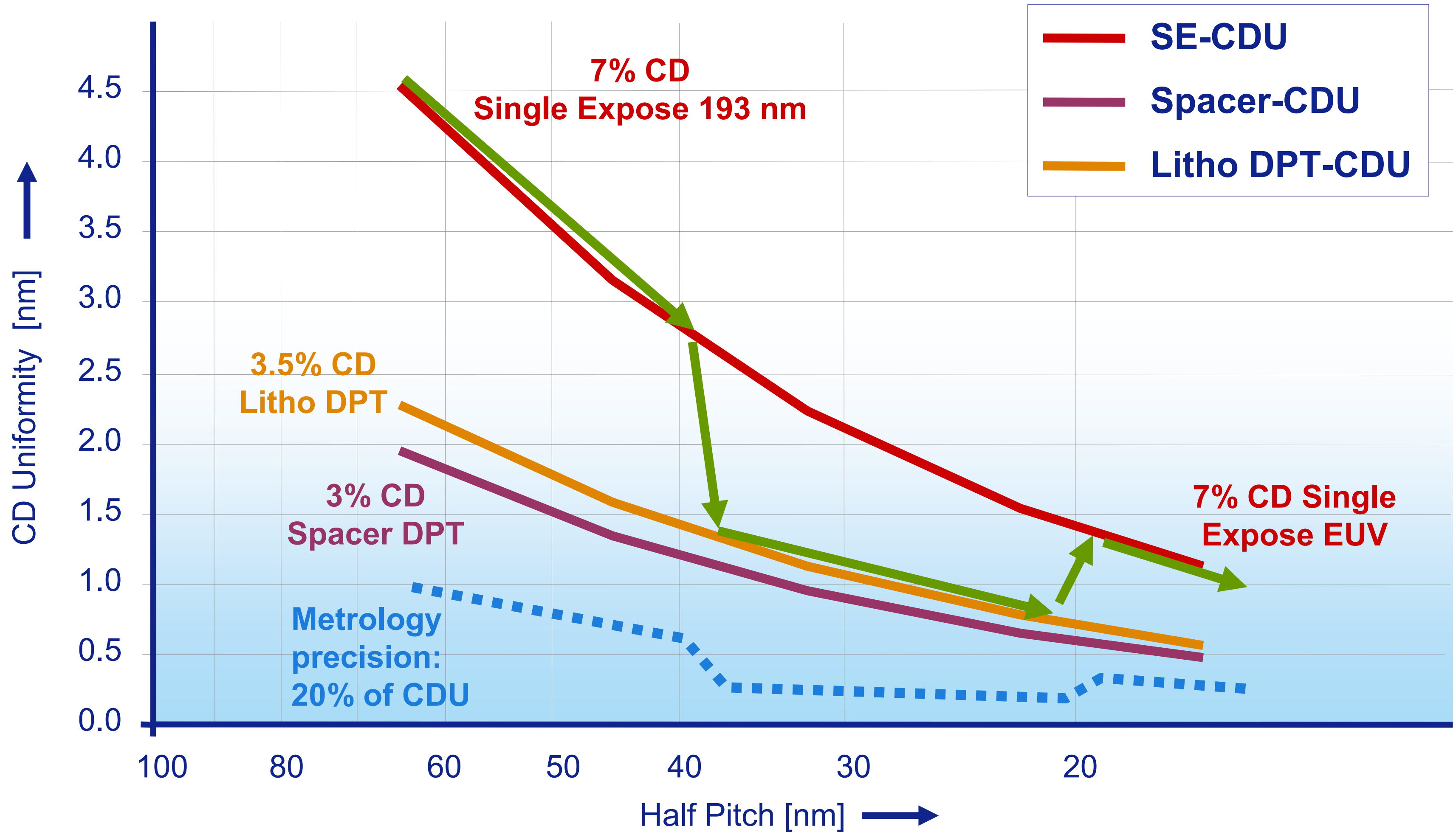
Spacer DPT



ASML

Required Litho CD Uniformity vs Half Pitch

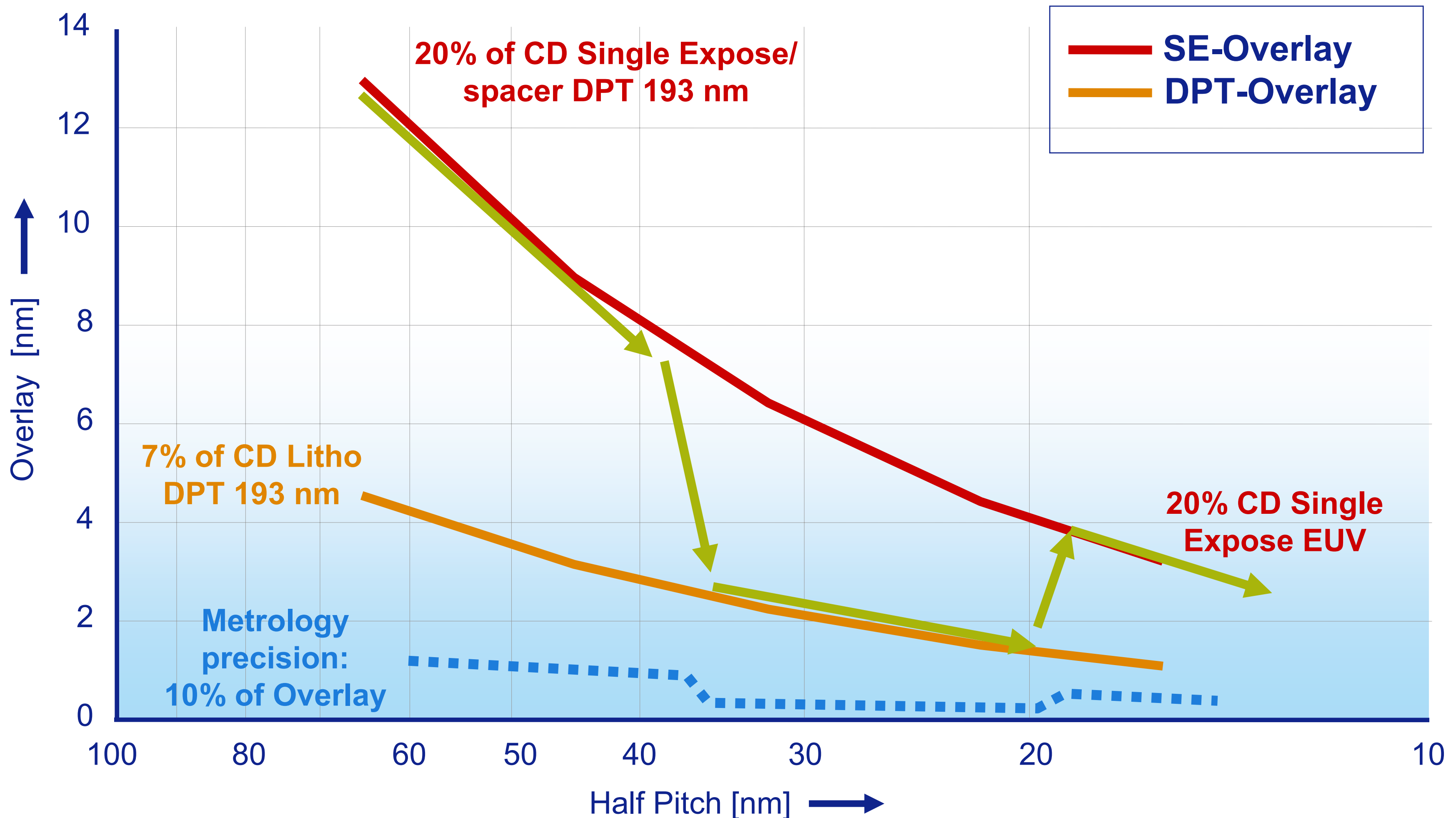
DPT drives need for significant improvement in CDU



ASML

Required Litho Overlay vs Half Pitch

DPT drives need for significant improvement in Overlay



ASML

Lithography Requirements Summary

DPT requires improved overlay & imaging, as well as higher productivity

Litho exposure equipment parameter as percentage of CD	Single exposure	Litho double patterning	Spacer double patterning
ΔCD	7%	3.5%	3%
Overlay (depending on DFM)	20%	7%	7-20%*
#mask steps	1	2	2-3
# process steps relative to single exposure	1	2	3-4

Requires improved productivity for CoO

Requires improved imaging & overlay control

* Depending on the amount of "Design For Manufacturing" effort

ASML

Outline

- Lithography Requirements
- ASML Holistic Lithography Solutions
- Conclusions

ASML

DPT Requires Holistic Litho Optimization

Combination of Computational and Wafer lithography

Mask definition

Illumination setting

Device pattern

Mask making

New NXT Platform for Lithography

Printed wafers

Scanner settings

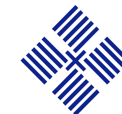
Metrology

Measuring CD & Overlay

Scanner-to-pattern tuning

Computational Litho

Wafer Litho



NXT:1950i Innovations for Superior Overlay & Imaging at 200wph

NXT is extendable with field upgrades

Reticle Stage with Improved Dynamics

Improved lens performance & control

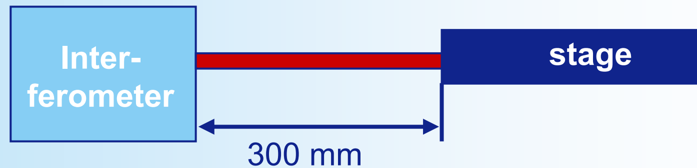
Planar wafer stages

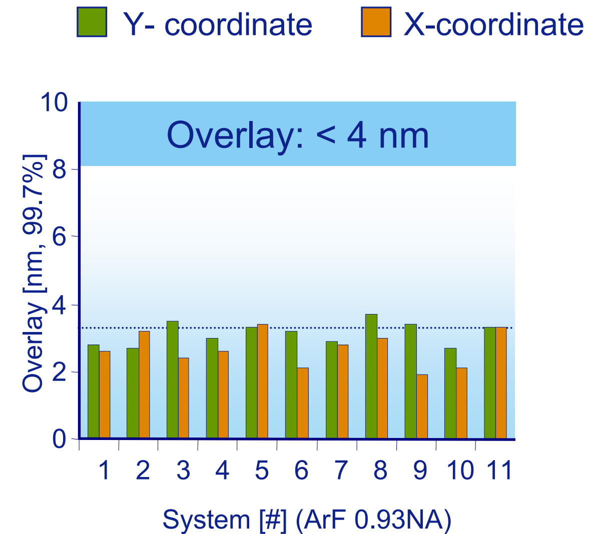
Grid plate position measurement (encoder)

ASML

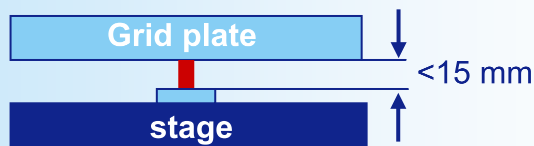
NXT wafer stage metrology impact on overlay

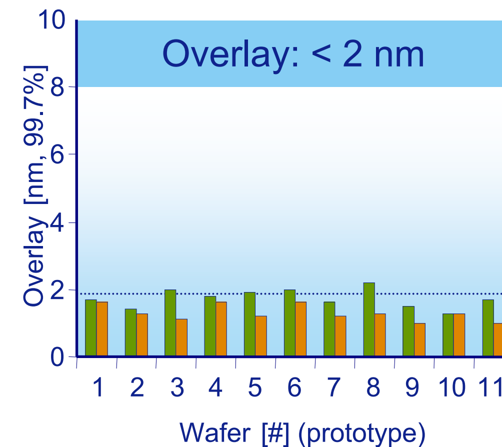
Current stage metrology





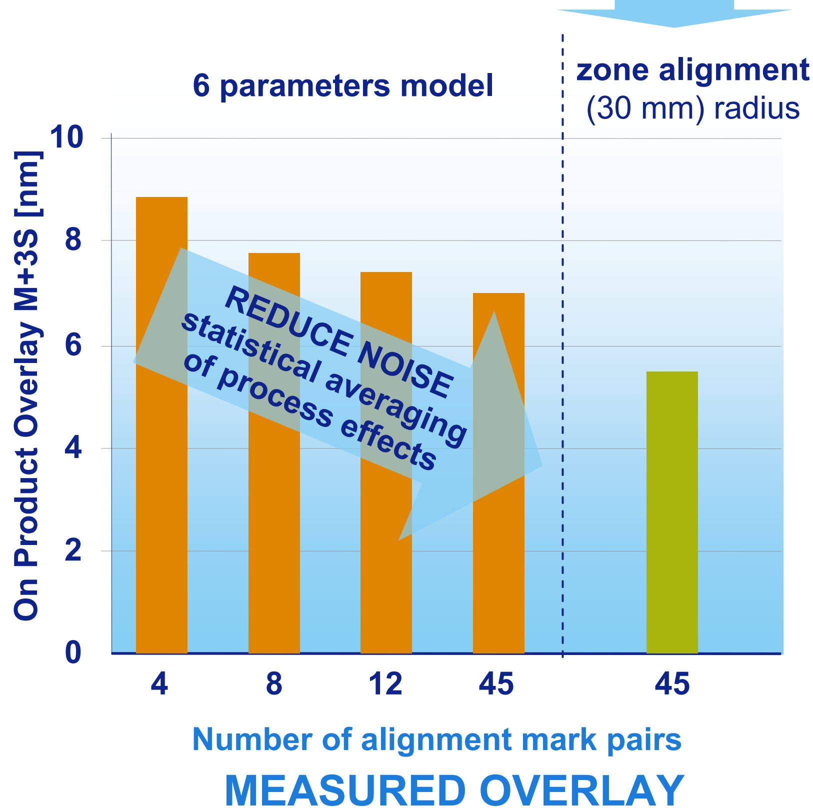
Improved metrology



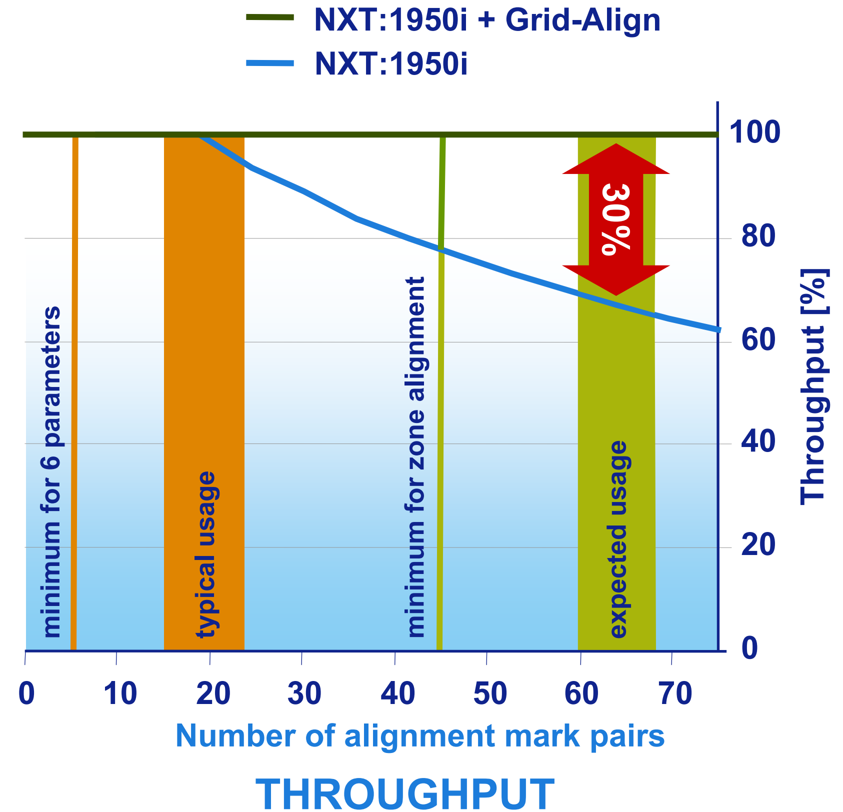


NXT: improved overlay at high throughput

scheme robust for grid deformations



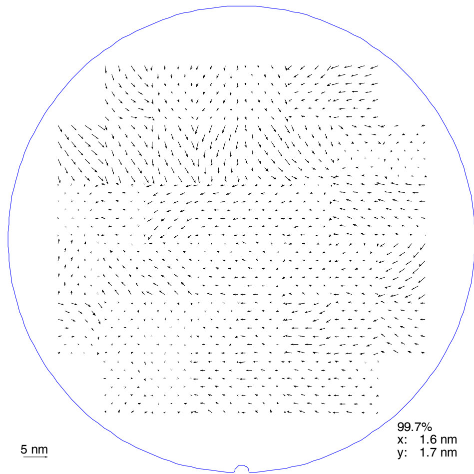
MEASURED OVERLAY



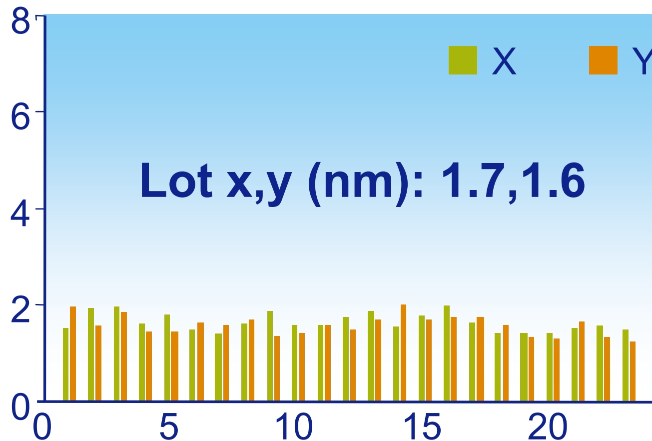
THROUGHPUT

NXT innovations bring immersion overlay < 2 nm

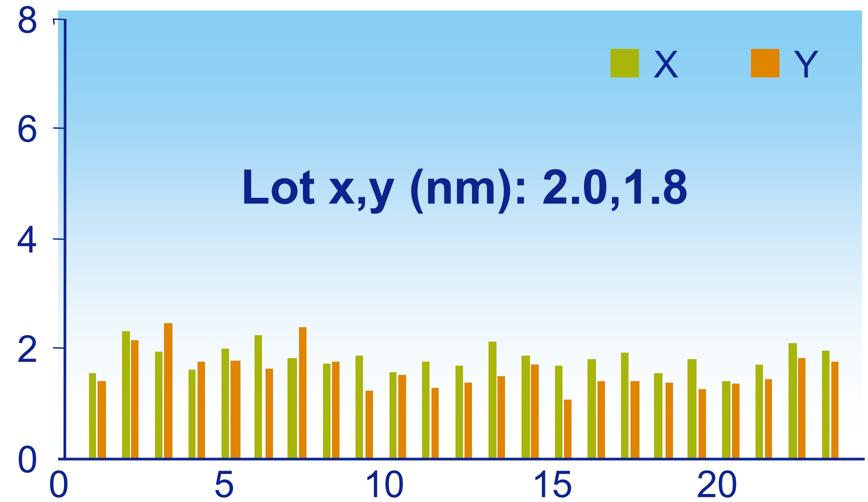
x, y : 1.6, 1.7nm



1 day overlay



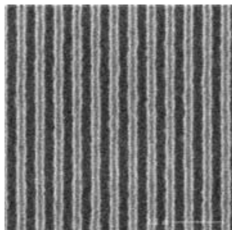
3 day overlay

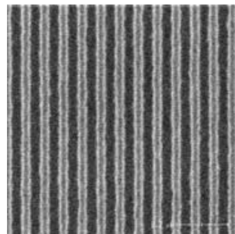


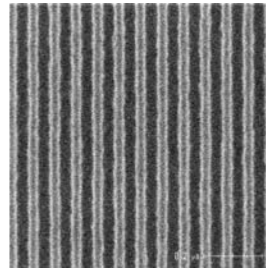
ASML

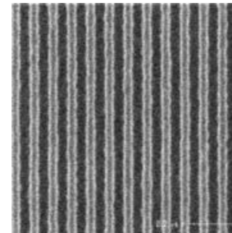
Ultimate half pitch at 1.35NA: *36.5 nm*

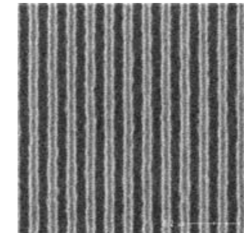
Large process window with 10% EL and 500nm DOF

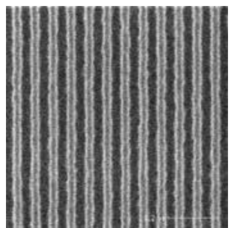

F=-0.21um

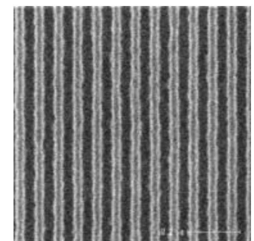

F=-0.12um


F=0.0um

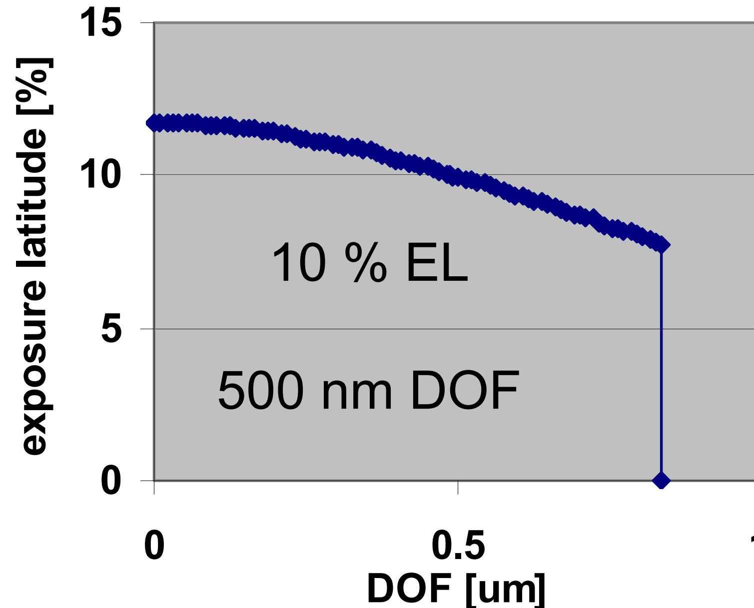

F=0.12um


F=0.21um


F=-0.3um


F=0.3um

k_1=0.255!



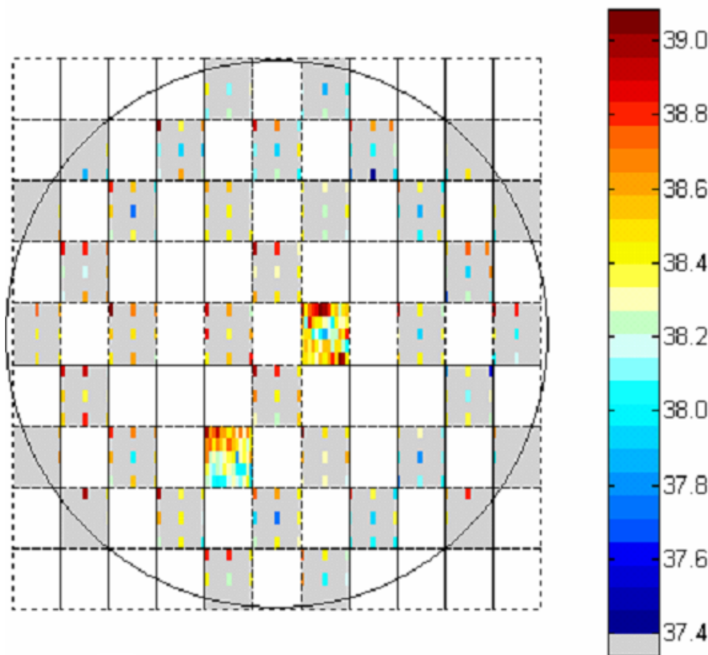
NA=1.35
σ=0.989/0.913
Dipole-20 degree
X Y polarization
6% att. PSM

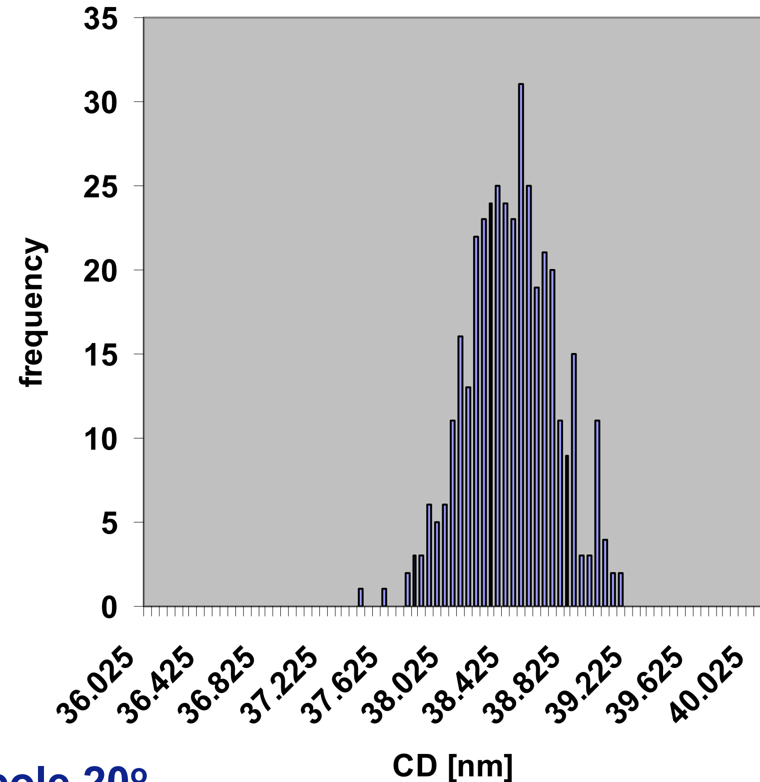
ASML

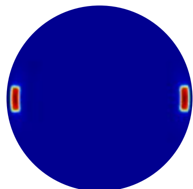
CD uniformity (3σ) below 0.9 nm with extreme dipole

38-nm dense lines measured CD uniformity

Full wafer ***CDU = 0.87 nm*** without reticle and process correction



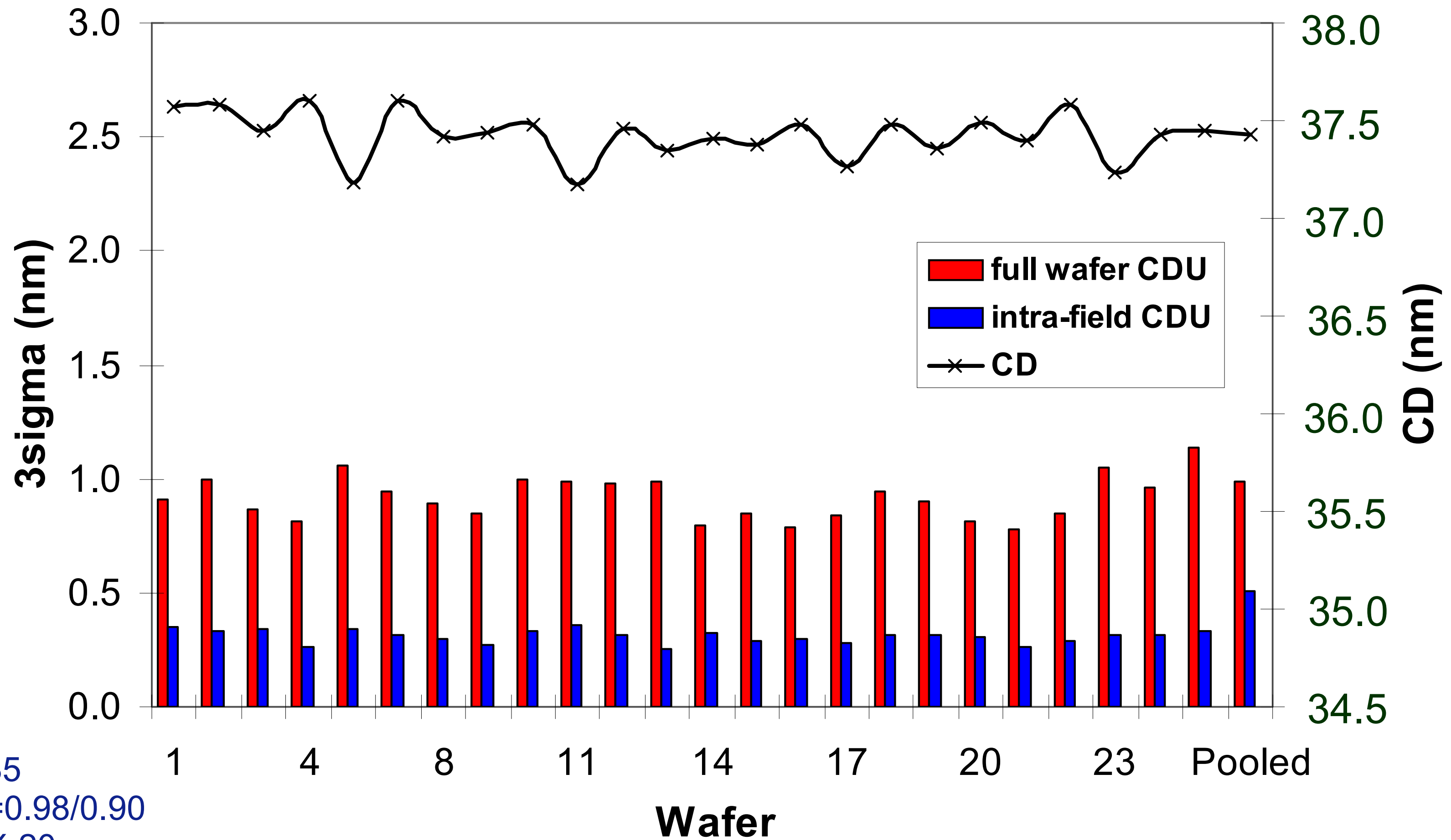




Settings: 1.35 NA with dipole 20° and sigma inner 0.90, sigma outer 0.98

ASML

Through lot wafer to wafer variation CDU <0.3 nm
38-nm dense lines with dipole illumination



NA=1.35
Sigma=0.98/0.90
DipoleX-20
TE-polarized

No correction applied for processing-profiles

ASML

ASML system throughput roadmap drives CoO

Wavelength
- Immersion
- ArF
- KrF
- i-line
- g-line

Wafer size
- 150 mm
- 200 mm
- 300 mm

150 mm stepper

200 mm stepper

200 mm scanner

300 mm NXT

300 mm AT & XT

ATP throughput [WPH]

0 40 80 120 160 200

1985 1990 1995 2000 2005 2010

Year of introduction

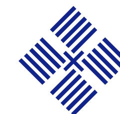
Source: ASML

ASML

NXT Immersion design : single digit defect level

45nm Pattern Defect Test (10 wafers)

KLA2800 metrology
Using top-coat TCX041
(SRCA 68 degree)

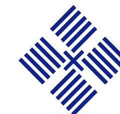


ASML

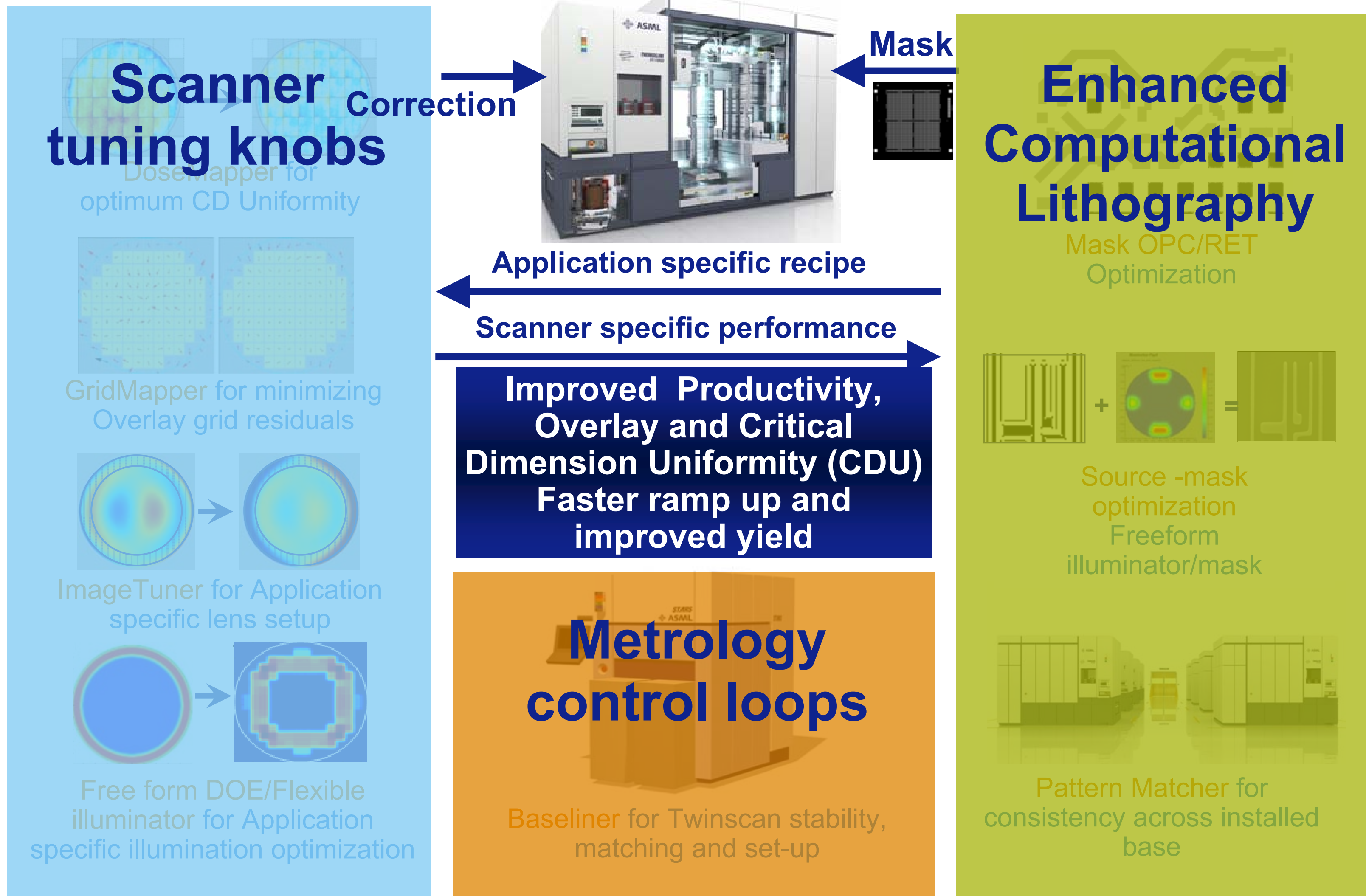
NXT Immersion design : single digit defects across multiple systems

45nm Pattern Defect Test (10 wafers) on 4 systems

KLA2800 metrology
Using top-coat TCX041
(SRCA 68 degree)



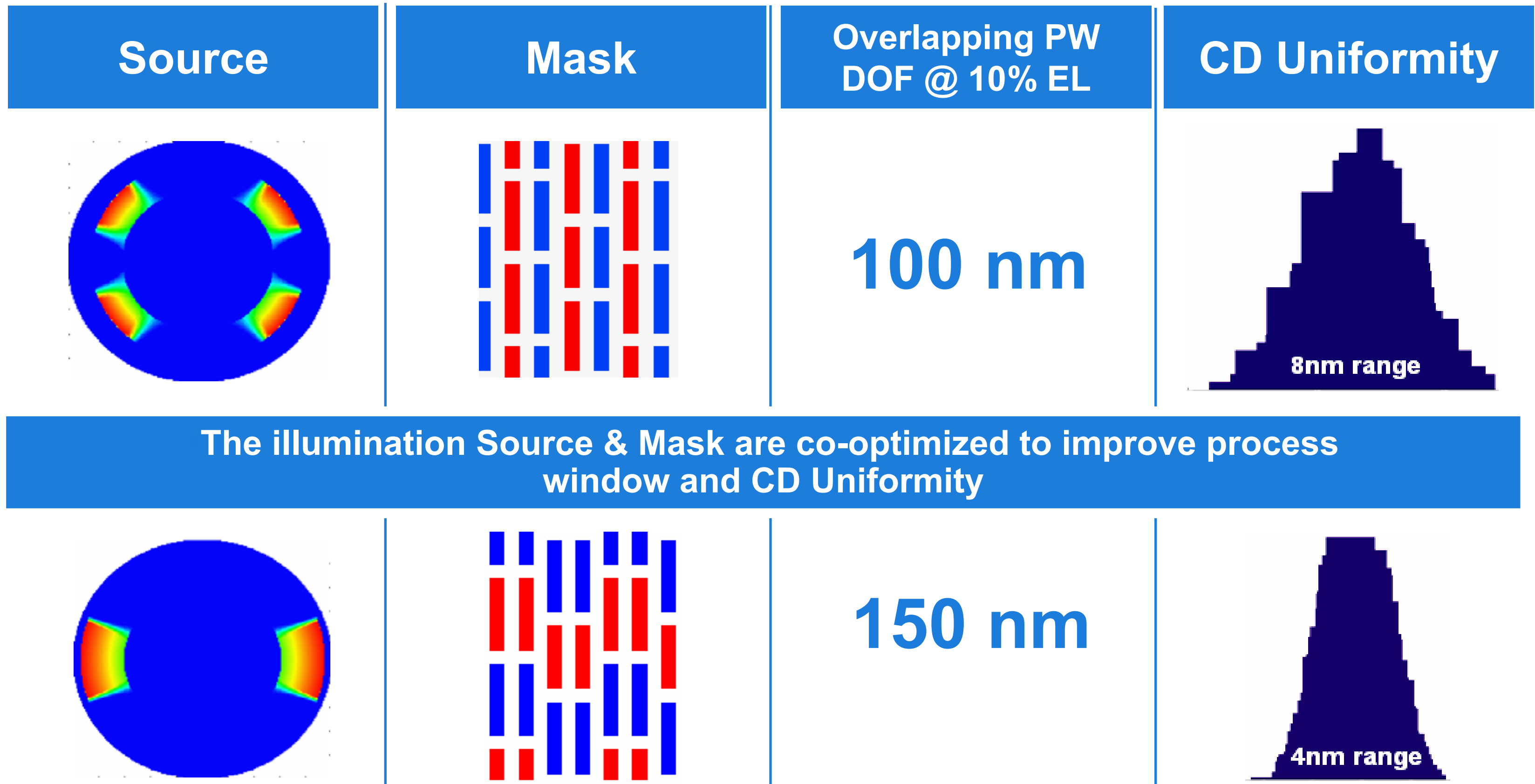
Holistic litho enables low k_1 / DPT applications



ASML

Co-optimization of source shape and pattern split

Enables optimum process window

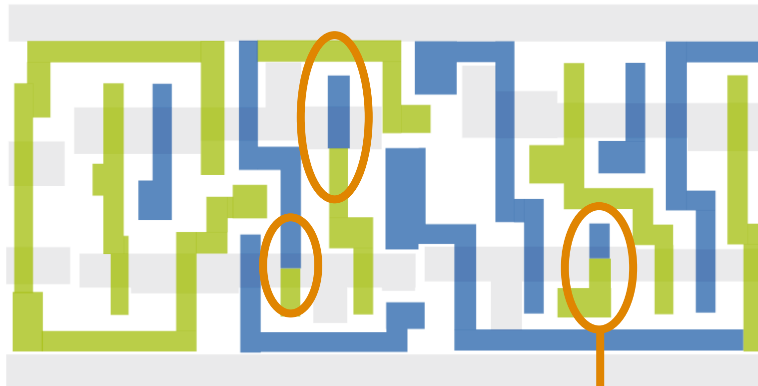


- By combining source expertise from ASML and mask expertise from Brion, enables larger process window with better CD Uniformity

Litho and application aware double patterning

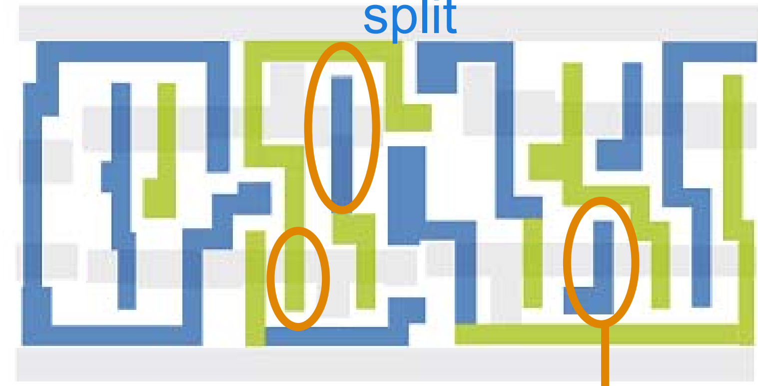
Example: 2D logic gate aware split & model based overlay stitching

- Standard



Poor pattern split on critical gate

- Gate aware split

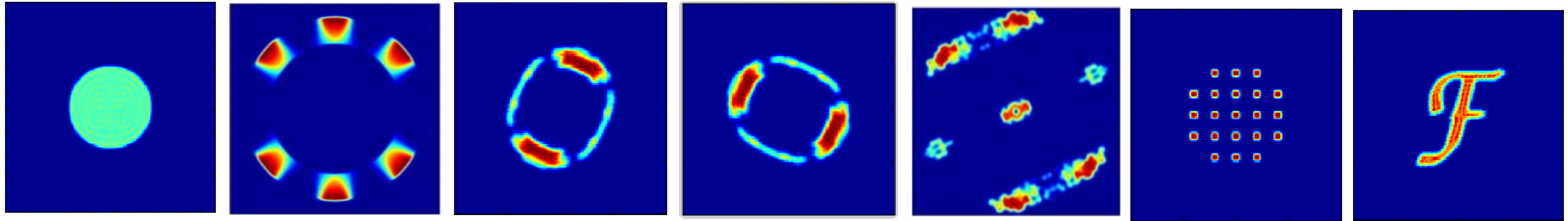


Optimal pattern split on overlay tolerant locations

- Diffusion
- Poly Split 1
- Poly Split 2

ASML

DPT requires a Fast & Flexible Source

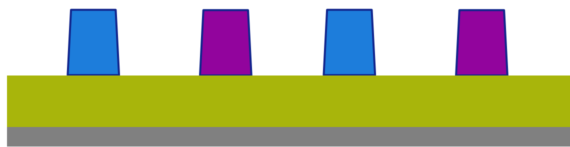


ASML FlexRay

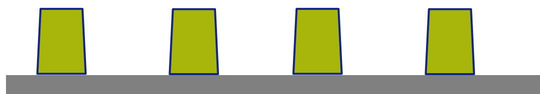
Holistic Litho Solution to optimize DPT CDU

Pitch =128 nm

Etch &2nd litho step



Etch



Pitch = 64 nm

Calculate Dose & Grid Map to optimize final CDU

CD metrology of lines & spaces

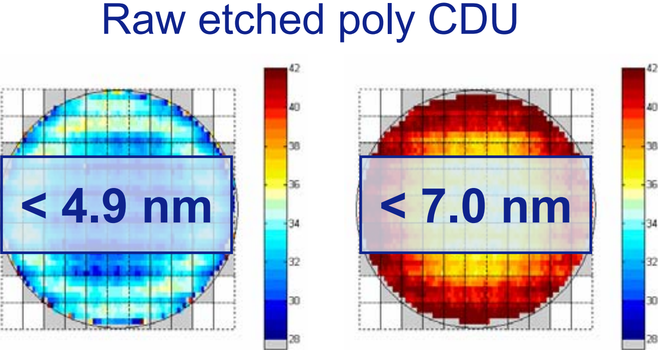
S2 L1 S1 L2 S2 L1 S1 L2 S2 L1 S1 L2

ASML

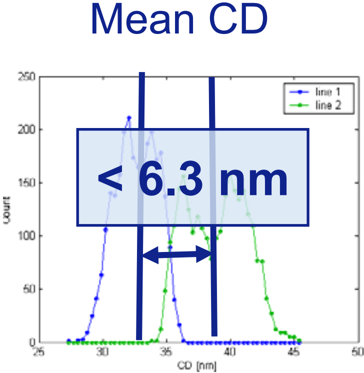
Litho patterning process control for CD and Overlay

Measurements of final 32 nm L/S using angular resolved scatterometry

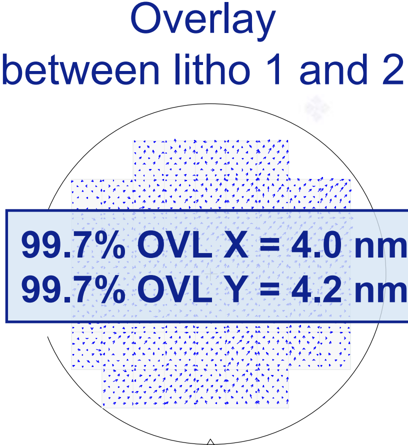
Raw etched poly CDU



Mean CD



Overlay between litho 1 and 2

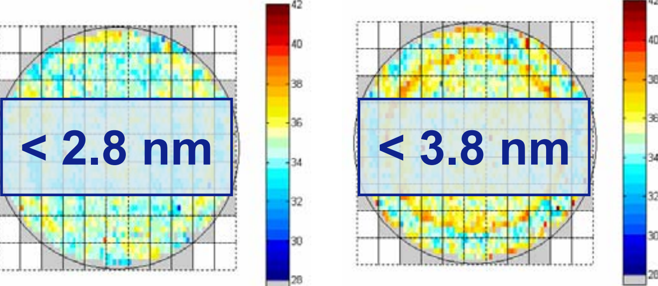


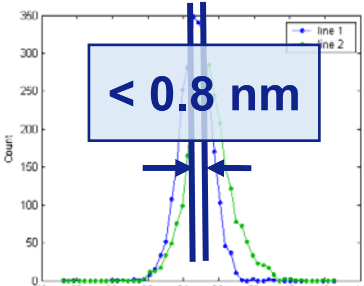
Line1 Line2

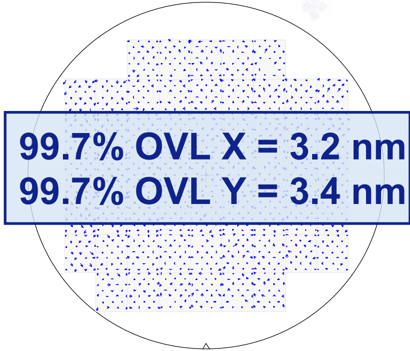
DoseMapper recipe

DoseMapper recipe

Optimum GridMapper recipe







DoseMapper corrected etched poly CDU

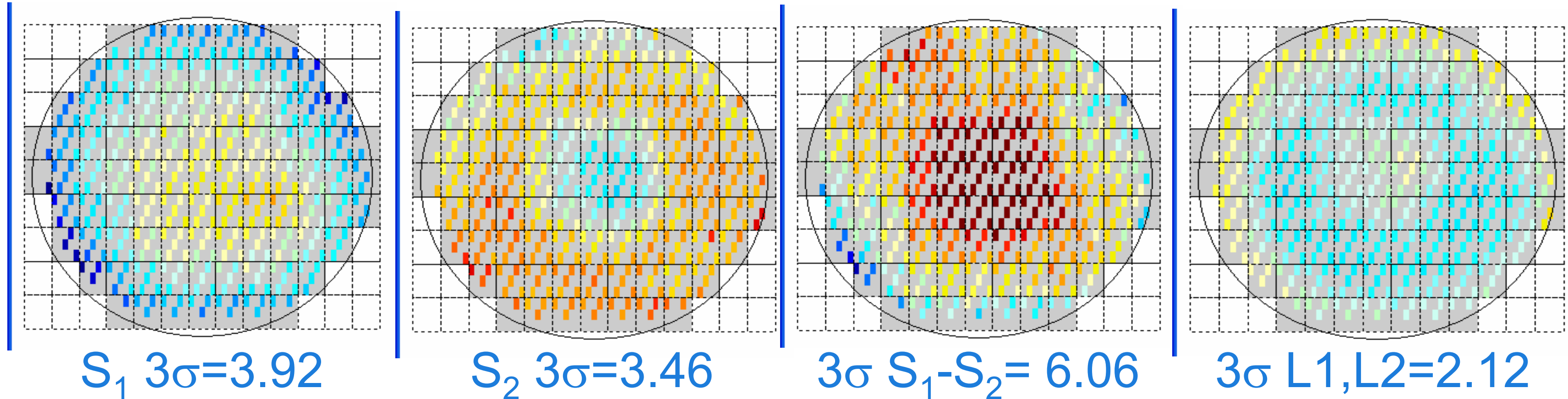
mean CD

Data generated in collaboration with IMEC

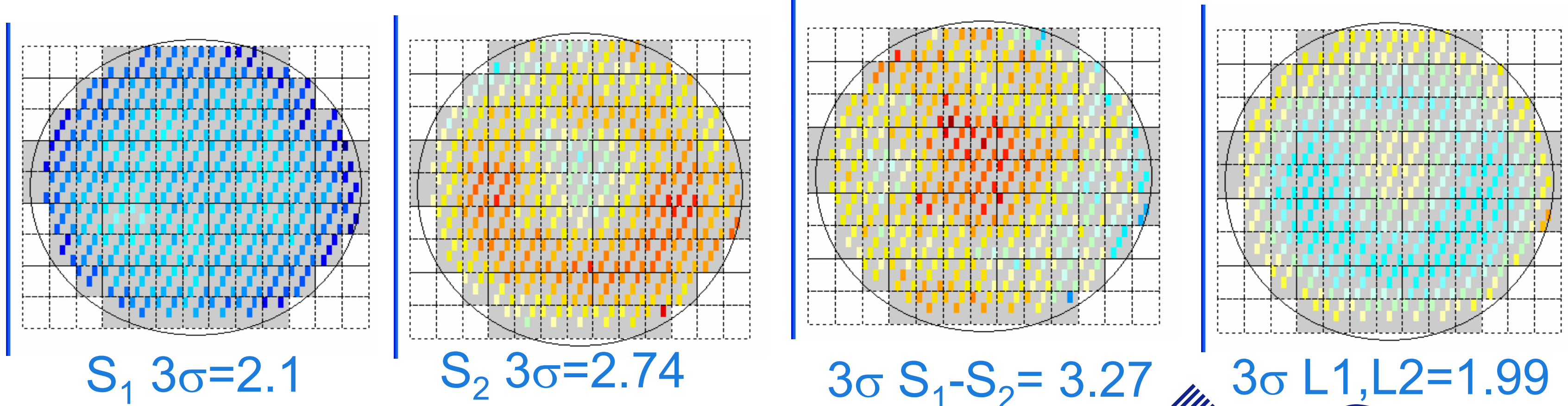
Spacer litho control improves wafer CDU

Measurements of final 32 nm L/S using angular resolved scatterometry

Uncontrolled



Controlled



ASML

Outline

- Lithography Requirements
- ASML Holisitic Lithography Solutions
- Conclusions

ASML

ASML Delivers Solutions to Drive Industry Shrink

DPT will bridge gap between single exposure 193nm & EUV

Resolution, "Shrink" (nm)

200
100
80
60
50
40
30

Logic
DRAM
NAND
AT:850
AT:1200
XT:1400
XT:1700i
XT:1900i
NXT:195
EUV
ASML Product Introduction
Immersion
Double Patterning
Holistic Litho

00 01 02 03 04 05 06 07 08 09 10 11 12

Year of Production Start

Source: ASML

ASML

Conclusions

- DPT will be used as a litho solution to enable future shrink as bridge between single exposure immersion & EUV
- DPT requires aggressive overlay & imaging requirements at high productivity
- NXT:1950 delivers required overlay & imaging at high tput to enable a cost effective DPT solution
- Co-optimization of source and pattern split via Brion products maximizes process window for DPT
- FlexRay delivers fast & flexible source shapes required for lowk_1 / DPT technology
- Holistic Litho optimization delivers solutions to optimize cdu & overlay to meet future lithography requirements

THANK YOU!