“Speed is the key”
Last words of many daredevils

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SEMATECH/IBM

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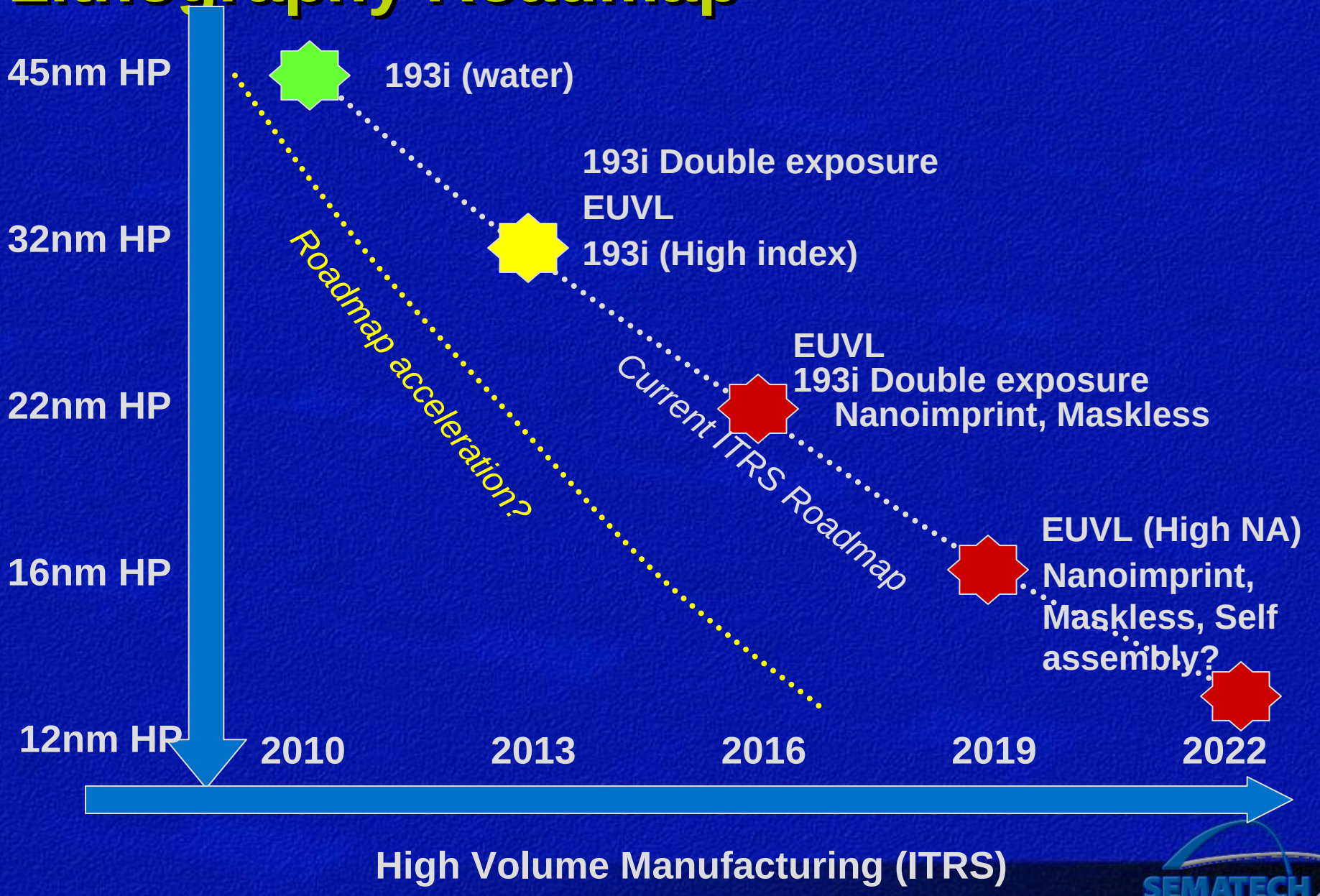
Accelerating the next technology revolution.

Outline

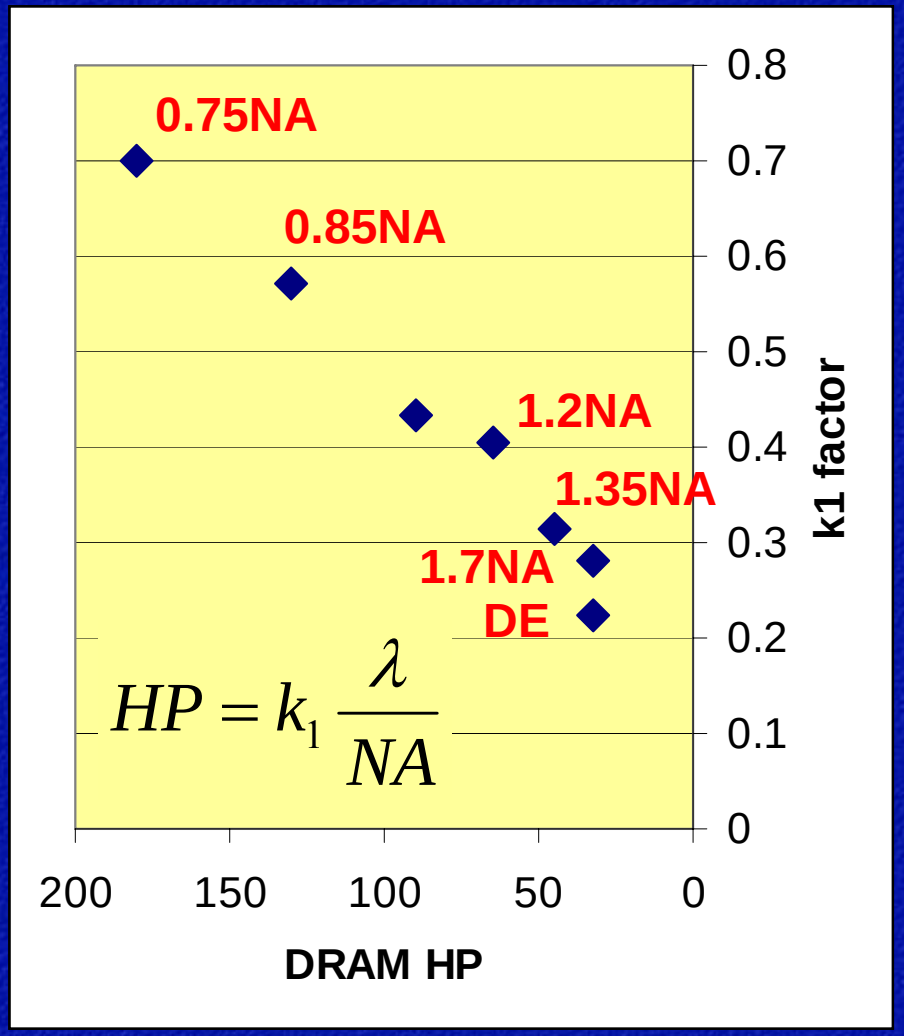
- Litho trends
- Scaling by wavelength and process
  - 193i
  - 193 Double exposure
  - EUVL
- Process complexity and cluster productivity

Lithography Roadmap



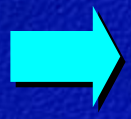
Lithographic Scaling: History

- For 193nm litho, process complexity scaling has been required at each new node even with improvements with NA
- Over 4 technology generations, NA has improved ~1.8x while half-pitch has scaled 4X

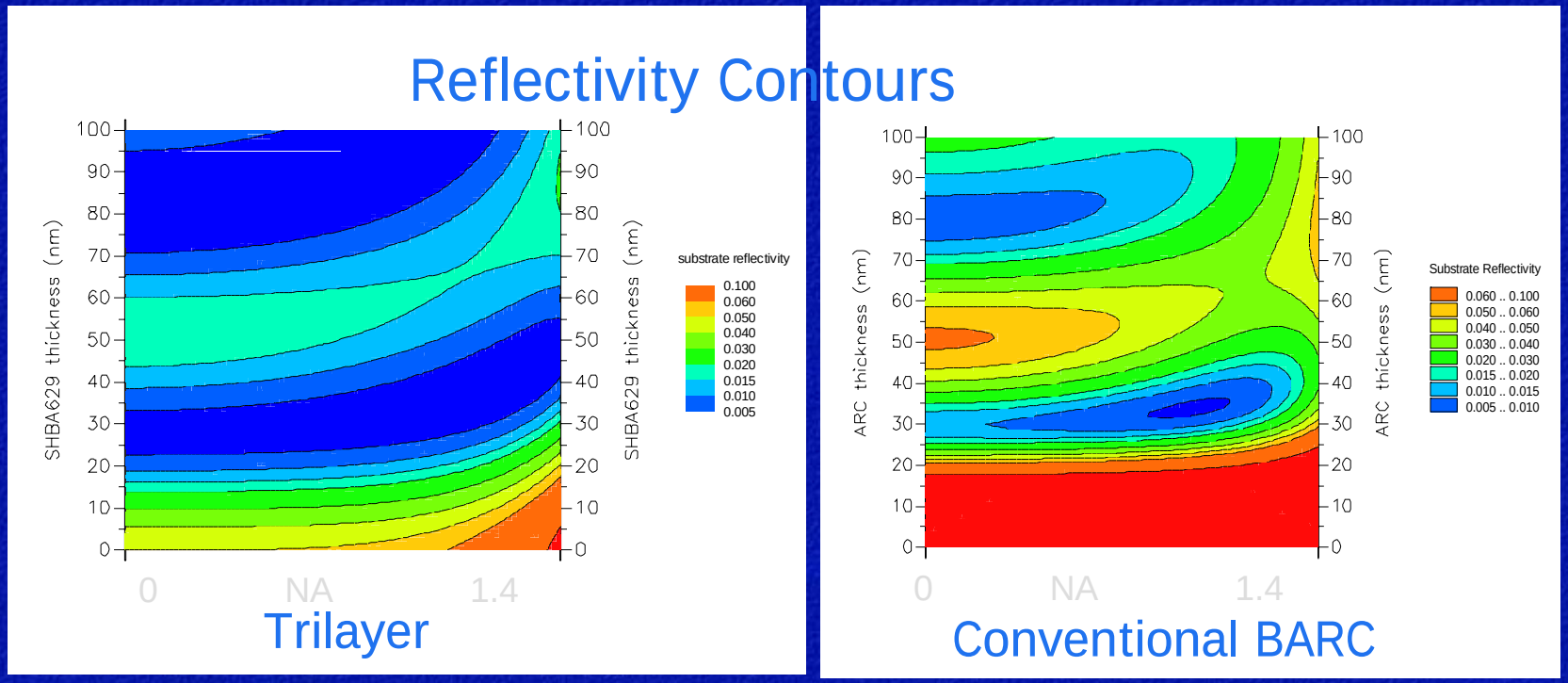


Cost of Scaling: Nothing Comes for Free

- Wavelength
  - Lasers: 248nm -> 193nm -> 157nm -> “13nm”
  - Optics: Fused silica -> CaF_2 -> Mo/Si ML
  - Resist materials
- Numerical aperture
  - Lens size / complexity
- Process complexity
  - Resolution enhancements (mask complexity)
  - Illumination optimization
  - Film stack improvements



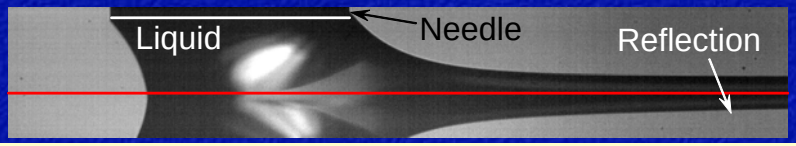
Hyper-NA Reflectivity

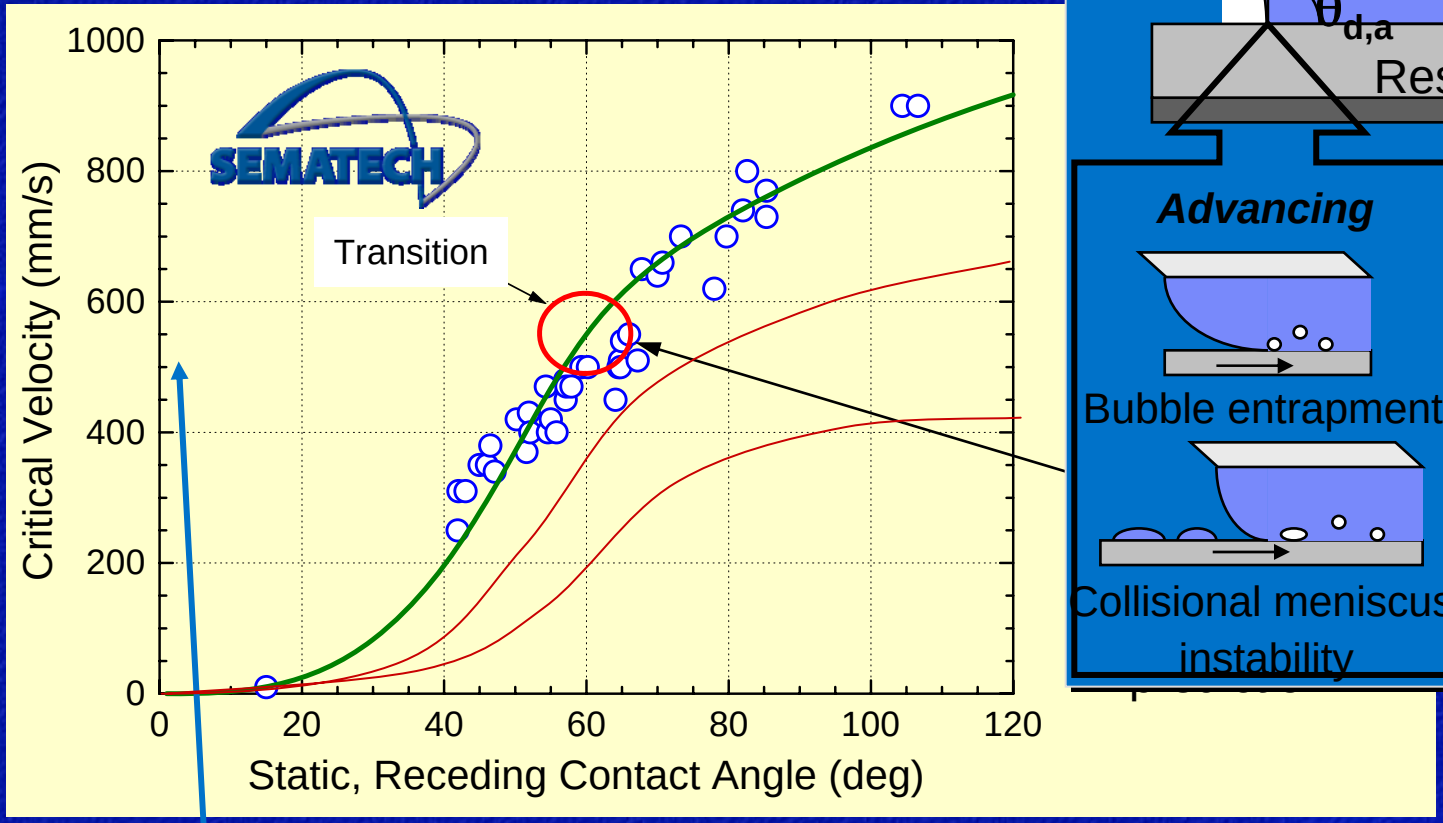


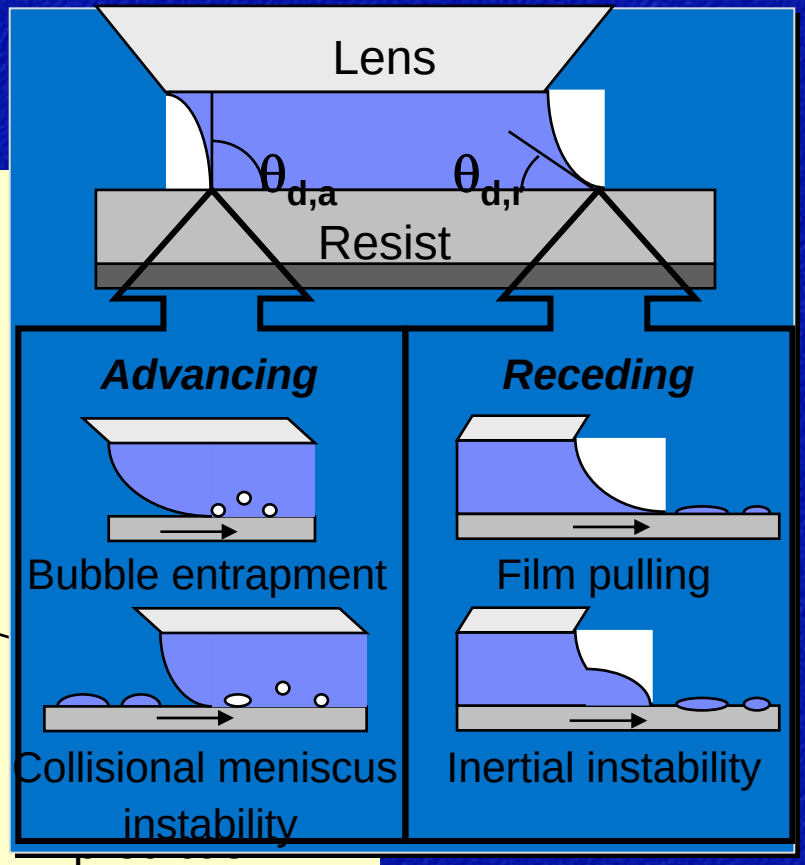
Reflectivity curves from George Gomba (SPIE 2007)

With single layer BARC, reflectivity control is impossible at hyper NA for multiple pitches. Mutilayer BARCs are required (with multiple coat steps)

High Speed Scanning with Immersion Fluids



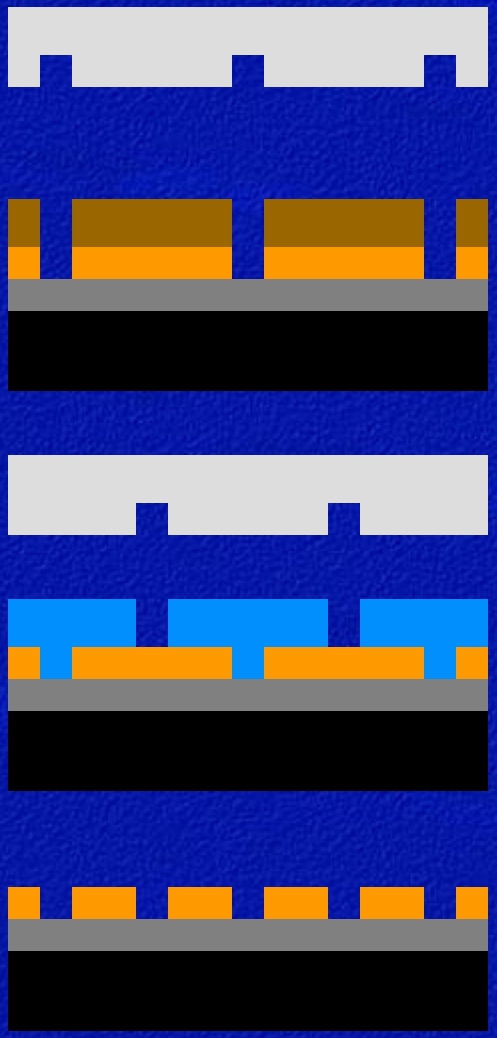




Critical velocities are close to high throughput scan speeds and decrease with increasing viscosity and decreasing surface tension

Double Patterning Steps

Dual Trench



Mask 1

Print trenches and etch hardmask

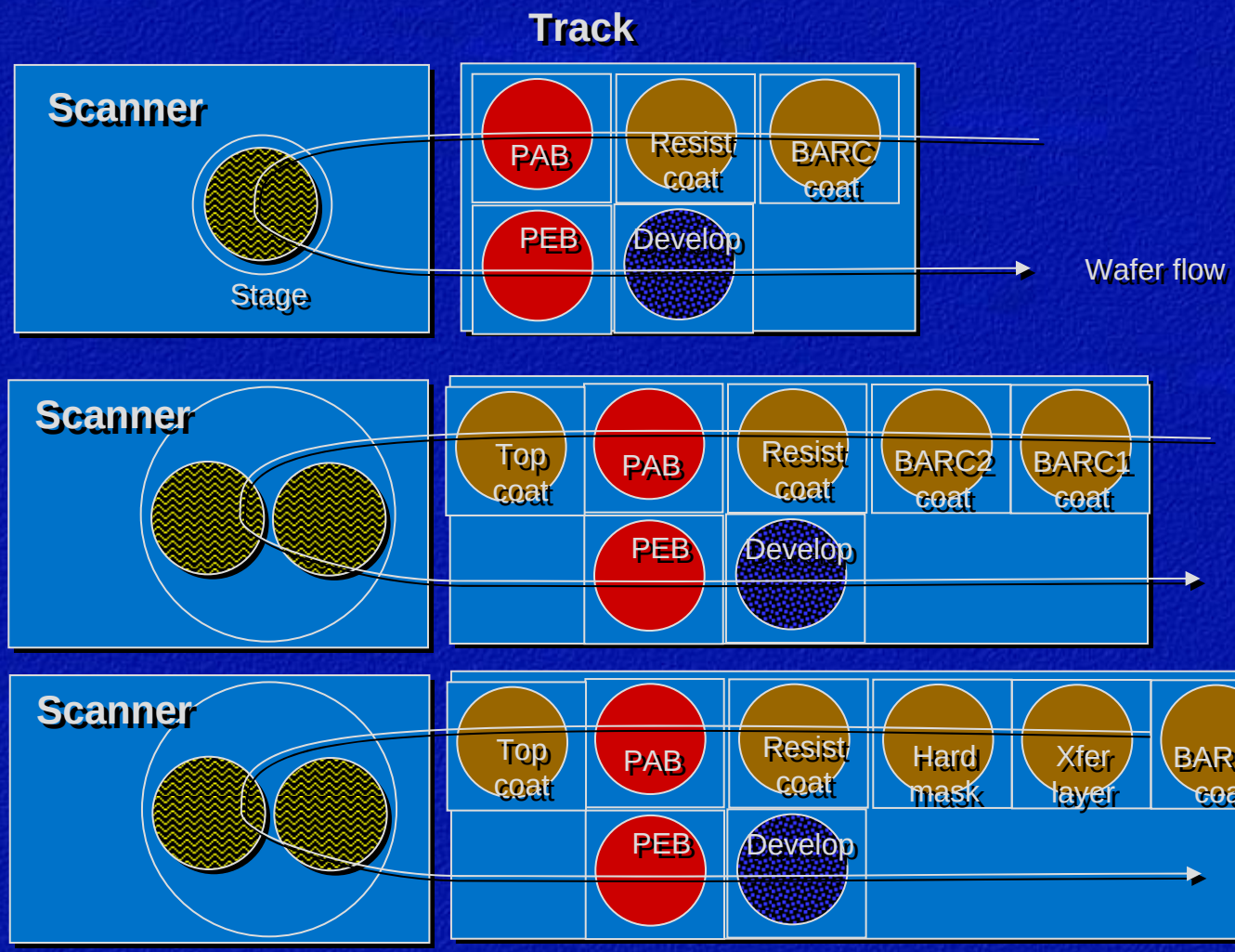
Mask 2

Strip first resist and coat and expose second resist

Etch hardmask and strip second resist

2 resist coat steps
2 resist develop steps
1 additional intermediate etch

Process Complexity Effect on Litho Cluster



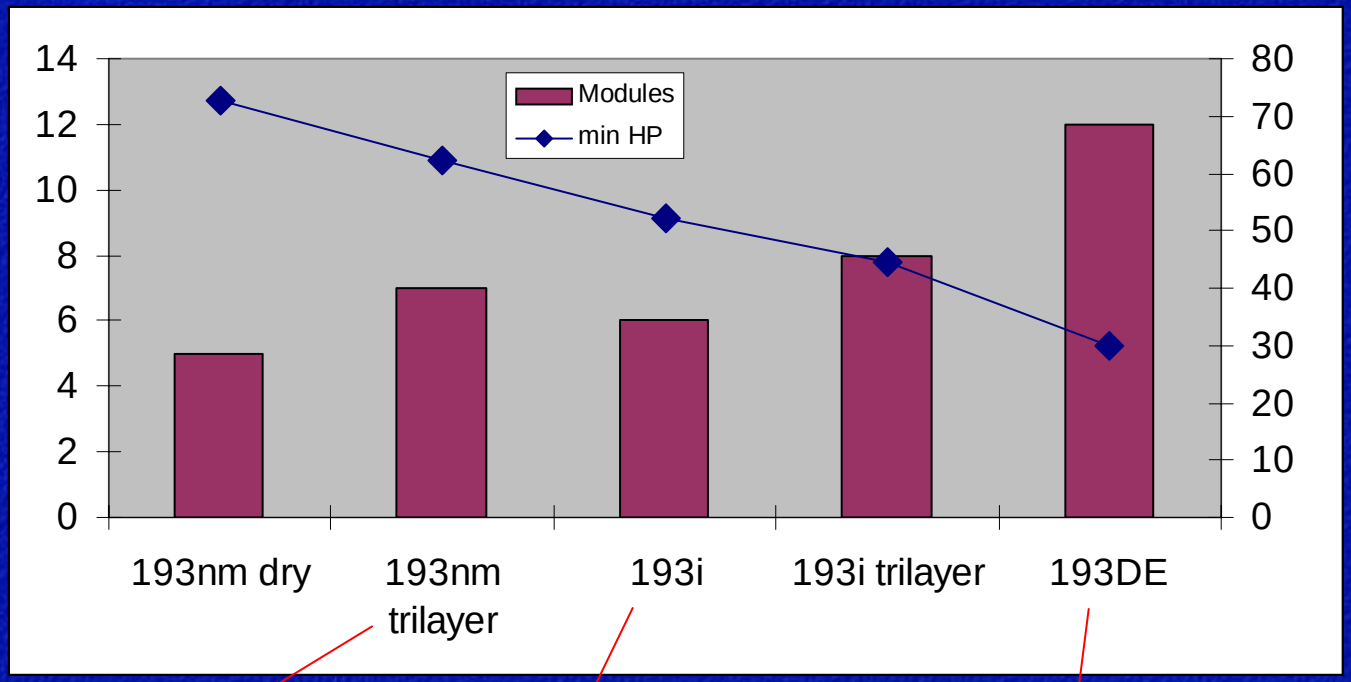
Single exposure, low-NA

Single exposure, Immersion, hyper-NA

Double exposure, Immersion, hyper-NA

Process Complexity: Track steps

- Process solution could require >2X more process steps



Improve DoF and etch selectivity

Topcoats for surface wetting control

Hardmasks and transfer layers

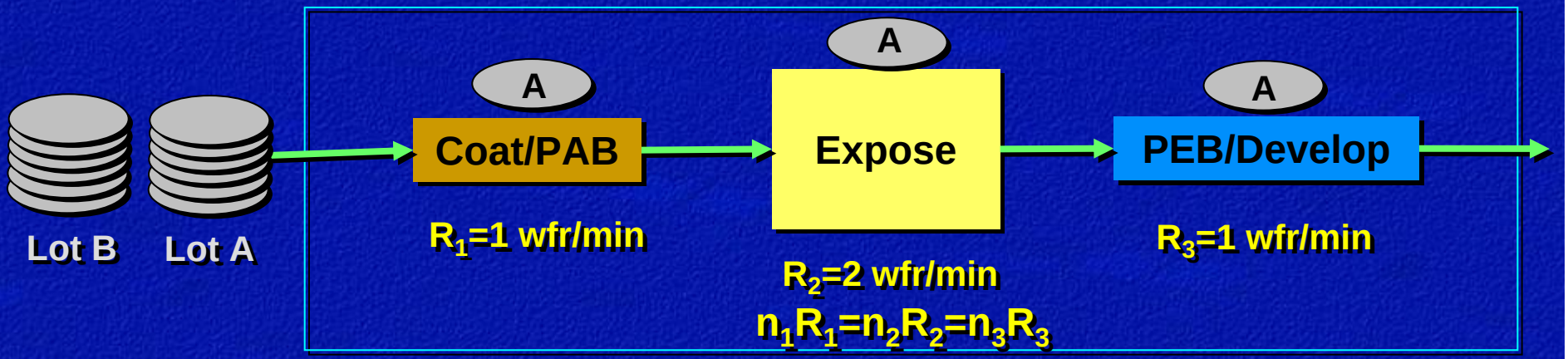
Typical 193nm Track Requirements

- From Paul Luehrmann, ASML (2005)
  - Includes extra modules for throughput

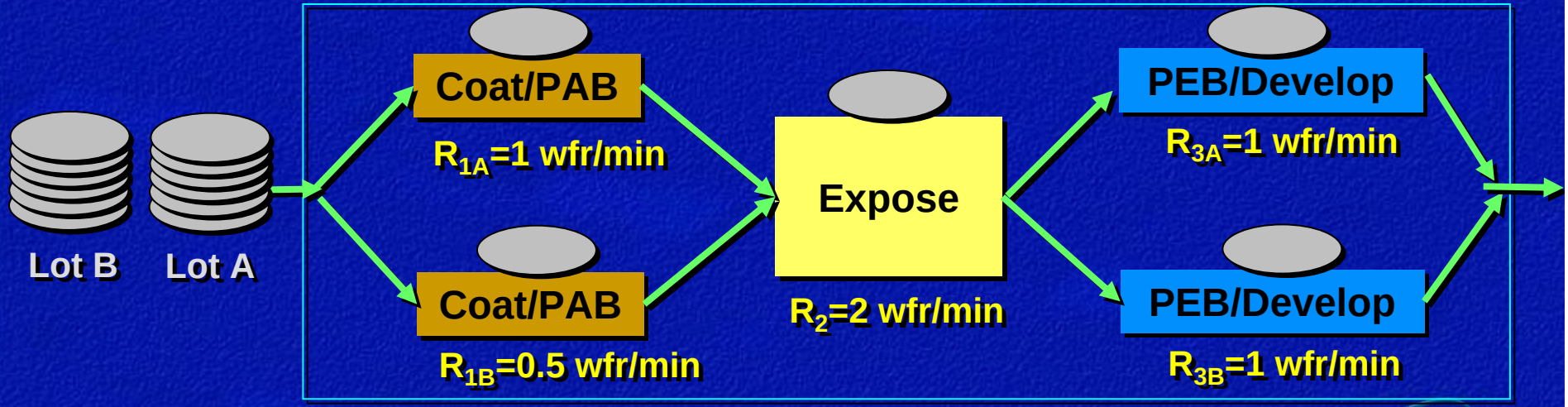
	BARC	Resist Coat	Develop	TARC	Solvent
Dry 193nm	3	3	5		
Low leach rate 193i	3	3	5		
Resist + topcoat (developer soluble)	3	3	5	3	
Resist + topcoat (solvent soluble)	3	3	5	3	3

Litho Cluster Productivity

Simple one process scanner/track

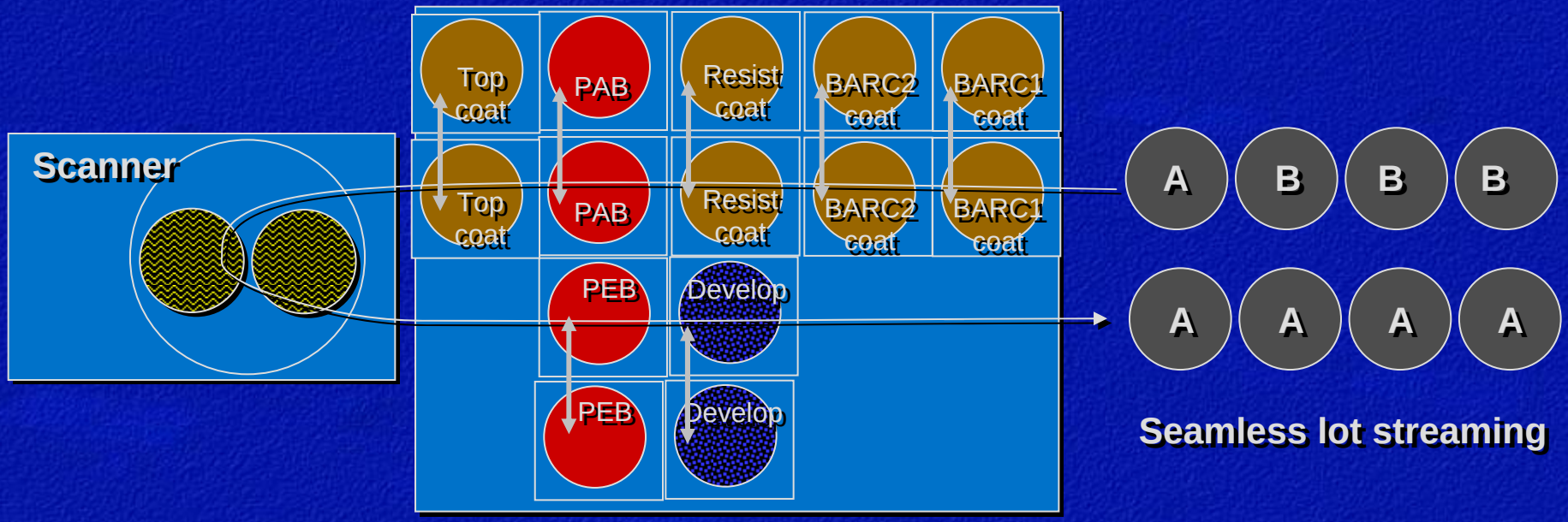


Multi-process scanner/track



High Productivity Litho Cluster

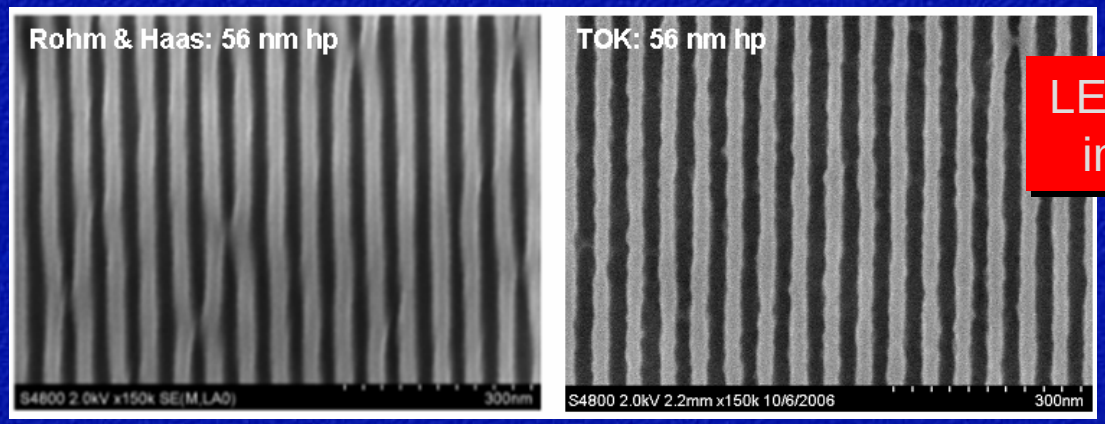
Each track step takes 1 to a few minutes per wafer
Each wafer takes <1 minutes per exposure step
Multiple coat/bake/develop stations required



Each cluster looks like a mini-fab!
Advanced material process flow required for high productivity

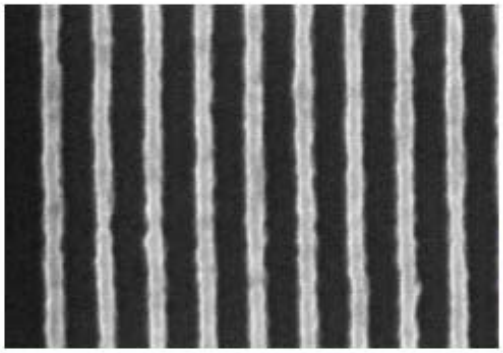
EUV Resist

- SEMATECH facilities demonstrate that simple film stacks are all that are needed to demonstrate resolution for EUV resists



LER/LWR needs improvement!

Images courtesy TOK and Rohm & Haas



Dose to size (50-nm 1:1) = 19 mJ/cm^2

Coded 22.5-nm:67.5-nm
Actual 22.7-nm:67.5-nm
LER 4.0 nm: L = 512 nm

courtesy of Seiya Masuda, FUJIFILM

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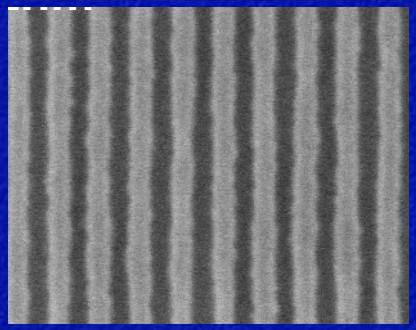

JSR Micro JSR MATERIALS INNOVATION

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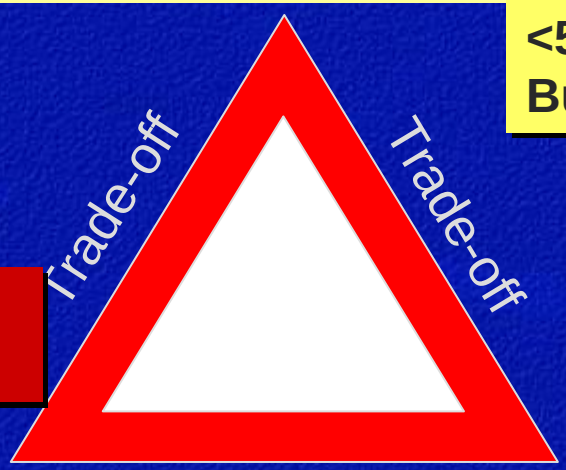
EUV Resist Technical Issues (32 nm hp)

- Simultaneously meeting Sensitivity, Resolution, and LER requirements remains challenging

Sensitivity: 10 mJ/cm^2

<5 mJ/cm2 demonstrated But LER high



~3nm is about the best LER shown anywhere

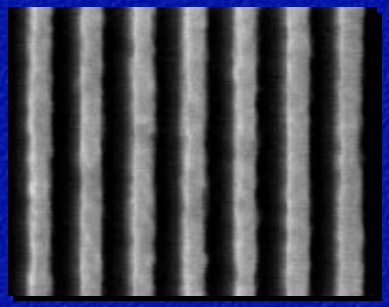
LER: 1.7nm

<28nm demonstrated, but dose is high

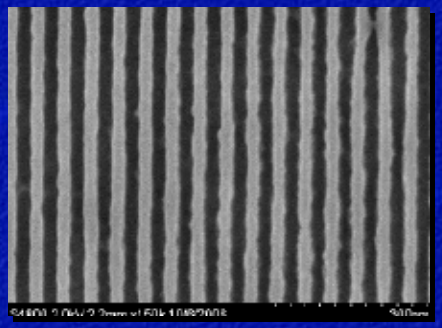
Resolution <32nm

- SEMATECH research is focusing on finding the ideal resist with good LER, Resolution, and Sensitivity

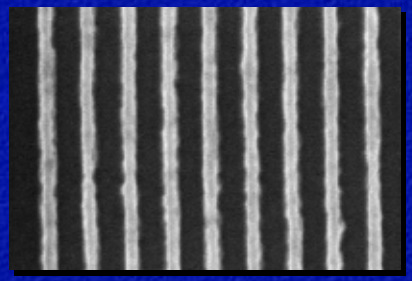
EUVL Resist Tradeoffs?



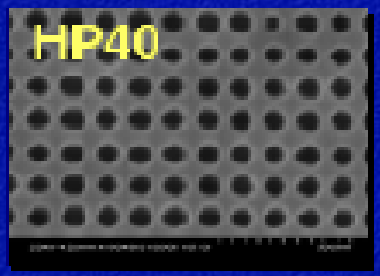
Good dense line resist ~20 mJ/cm^2 (today)



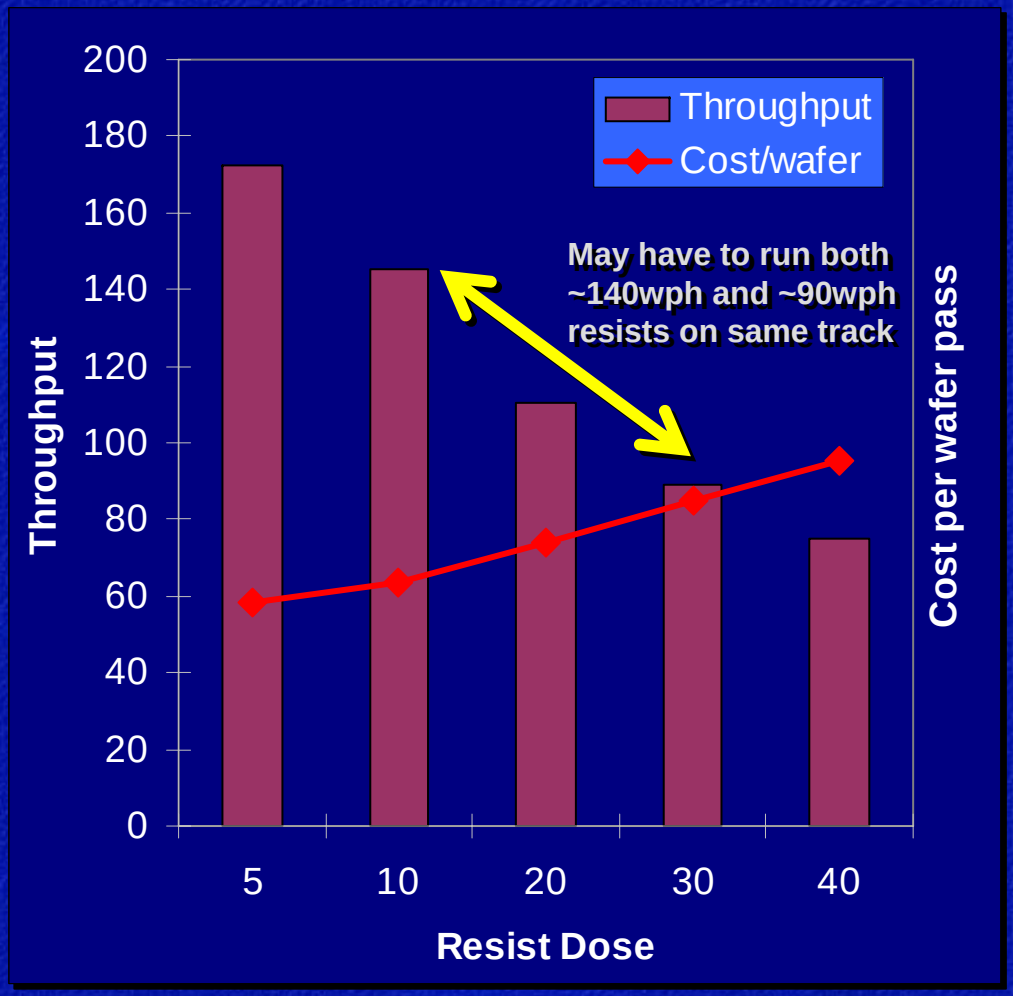
Low dose dense line resist ~12 mJ/cm^2 (today)



Gate resist (low LER) >30 mJ/cm^2 (today)



Contact hole resist >20 mJ/cm^2 (today)



EUVL is heavily photon limited
Optimizing resist per level may impact scanner throughput

Maintaining Productivity

- Scanner
  - May run 120+ wafers/hour
  - May run 60 wafers/hour (double exposure)
- Track
  - May need 5 process modules per wafer pass
  - May need 12 process modules per wafer pass
  - Modules may be different
- What is most efficient cluster?

Track of All Trades

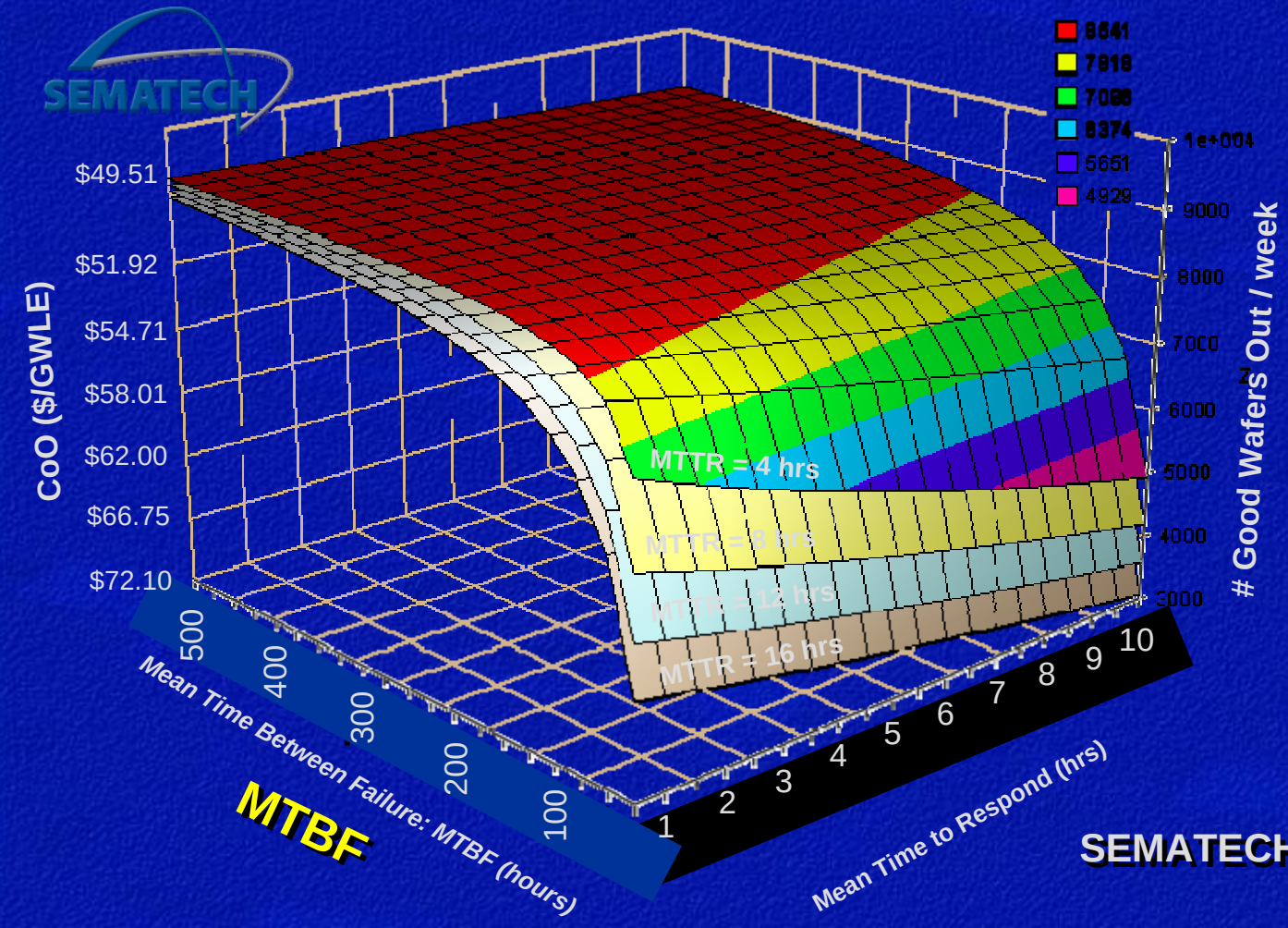
- From a productivity standpoint, the ideal track then should cover all process modules for full scanner throughput

High Productivity is Not the Only Metric

- Environment
  - Resists generally sensitive to environmental contamination
- Process variability
  - Very tight targets on CD uniformity and repeatability
  - Drives very tight control of PEB bake temperatures
- Defects
  - Very low defects required from wafer handling and processing
  - Immersion processes require additional control of surface properties
  - Double exposure wafers make two cluster passes for each device level
- Manufacturability
  - High uptime and good mean-time-to-recovery

Reliability, Availability, and Maintainability (E10-0403):

Mean Time to Respond vs. MTBF vs. MTTR



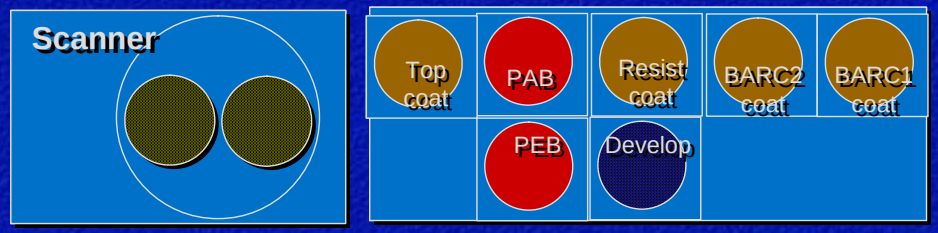
Low MTBF drives high litho cost because expensive cluster remains idle

SEMATECH CoO Calculations

From Phil Seidel (SEMATECH)

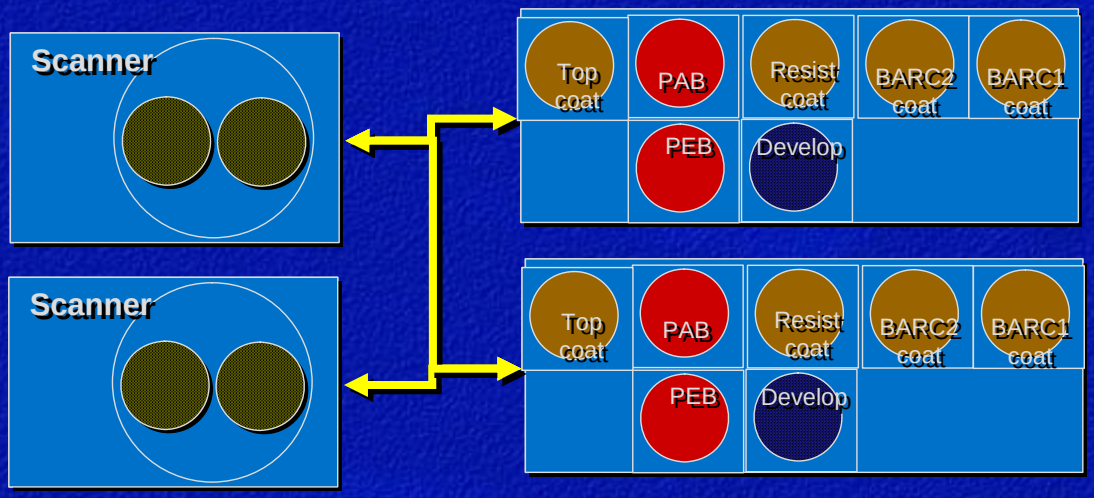
Linked?

Linked cluster



+ Less handling (defects)
+ Resists stay in closed environment
= Material handling / lot streaming within tool
- Productivity of cluster less flexible

Unlinked cluster



- More handling (defects)
- Resists exposed to environment
= Material handling / lot streaming outside of tool
+ Productivity of cluster more flexible

Summary

- Litho cluster productivity is an important driver of cost per good wafer level exposure
- Good wafer level exposures are determined by process capabilities and specific requirements of each technology
- Diversification of technology drives additional process and litho film stack requirements
- Customers want high throughput, but not at expense of flexibility or yield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