Scanner vs. Track
Don't forget about the materials!
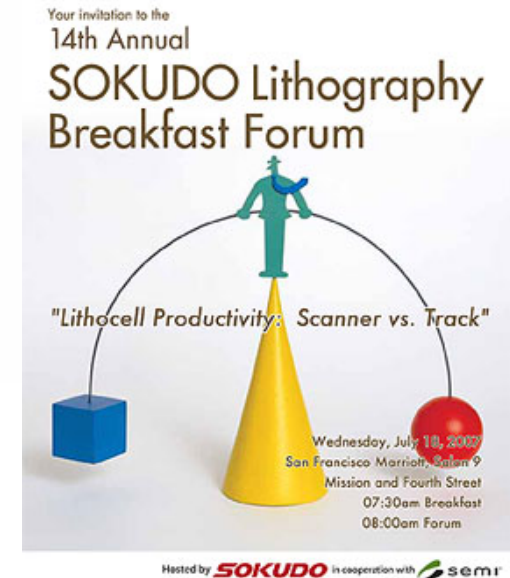
Sokudo/SEMI Lithography Breakfast Forum - 2007

Mark Slezak

The lithography battle
Scanner vs. Track

- Where do materials fit in the battle?

  - Who do we like better?

  - Materials are your friend!

- Other battles on the litho front

  - Topcoats vs. Non-topcoat immersion resists

- The Lithocell vs. Materials

Your invitation to the
14th Annual
**SOKUDO Lithography
Breakfast Forum**

"Lithocell Productivity: Scanner vs. Track"

Wednesday, July 18, 2007
San Francisco Marriott, Salon 9
Mission and Fourth Street
07:30am Breakfast
08:00am Forum

Hosted by **SOKUDO** in cooperation with semi

Who do we like???

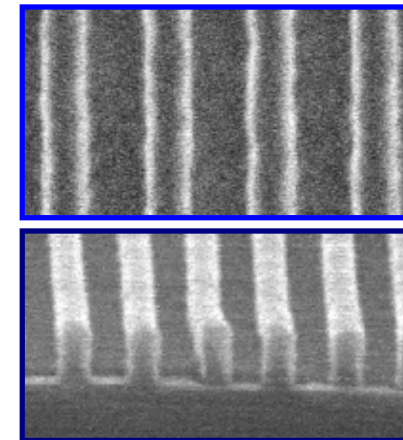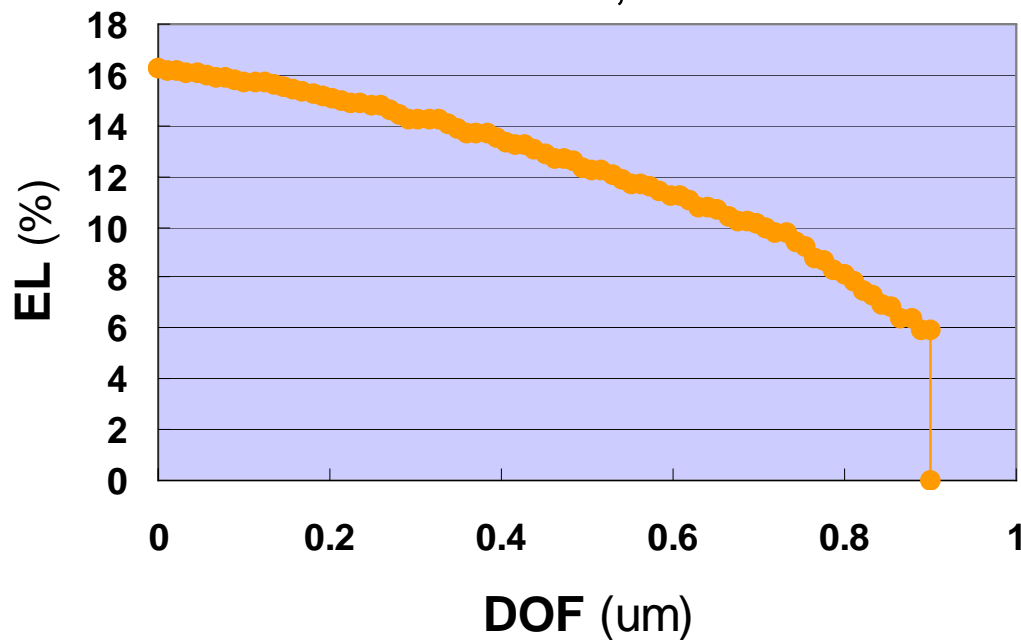|	Scanner	Track
Positives	▪ Higher Numerical Aperture ▪ Improve aerial image	▪ Bake plate uniformity ▪ Improved exhaust ▪ **Dummy Dispense**

Negatives	▪ Lots of rules…..
	  scan speed requirements
	  leaching specs
		▪ Lots of rules……
		  drain line compatibilities
		  outgassing
		  shot size reduction

It's not just a one way street

- We need to lean on each other:

    - **Scanner** → Aerial image
    - **Track** → Film thickness & bake plate uniformity

    - **Materials** → examples of how we carry our own weight
        - Advanced photoresists
        - TARCS
        - Topcoats
        - Others….

Materials are your friend

	Scanner	Tracks
Advanced photoresists	▪ Large depth of focus & exposure latitude	▪ Post exposure bake sensitivity

55nm 1:1, 1.0NA

LWR 4.9nm
PEBS ~1nm/C
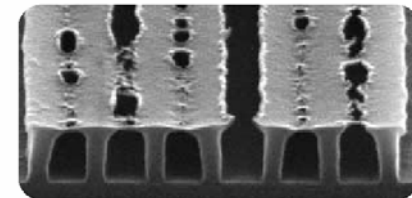
Materials are your friend

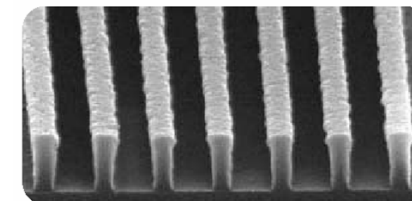|	Scanner	Track
TARCS	▪ Controls your leaky light ▪ Reduces outgassing	▪ Amine control ▪ Lower defectivity
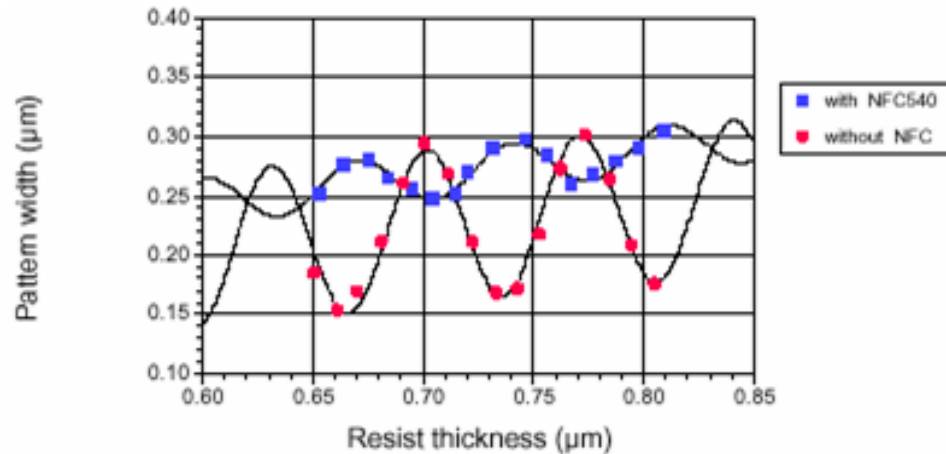
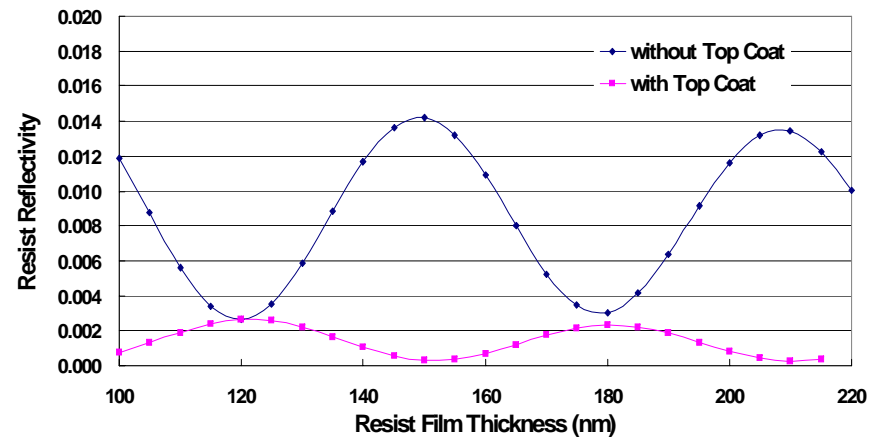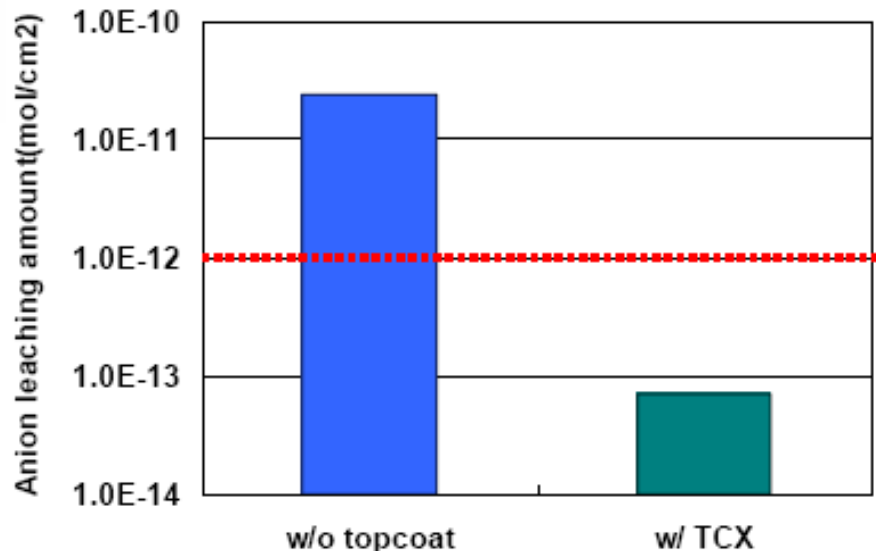**Environmental Stability**
60min PEB delay

No TARC

with TARC

Materials are your friend

	Scanner	Track
Immersion topcoats	▪ Minimizing leaching ▪ Helps w/ reflectivity control	▪ Sell more pumps and coater bowls

Materials are your friend

	Scanner	Track
Others: **Chemical Shrink**, DP, trilayer materials	▪ Relaxes pressure on resolution	▪ Sell more pumps and coater bowls

ADI: 90nmS180nmP

| -0.4 | -0.3 | -0.2 | -0.1 | 0.0 | +0.1 | +0.2 | +0.3 |

LWR:7.3nm
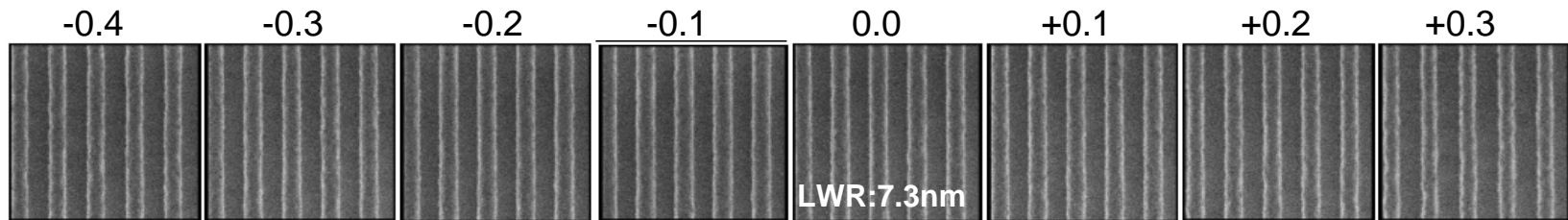
After Shrink: 70nmS180nmP

Chemical Shrink Material
20nm Shrink!!

LWR:6.8nm

70nmSpace (20nm Shrink)
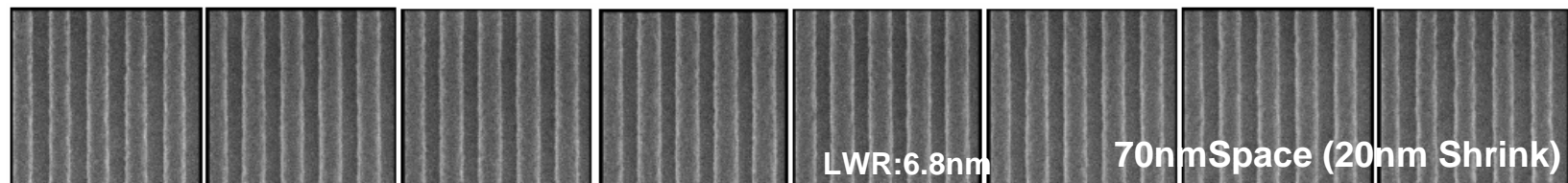
✓ **Excellent bake plate, coating uniformity, and other engineering controls**

Harmony

✓ **Good aerial image and other engineering controls**

✓ **Large process latitude, reflectivity control, and other process enhancement techniques**

Other battles on the litho front

Topcoat vs. non-topcoat: checklist

✓ Develop & scale-up topcoats → Done

✓ Support implementation into the 45nm node → On-going

✓ Build TC-less resist → On-going

✓ Prove which one is better → On-going

Topcoat design

Water/Air

Topcoat
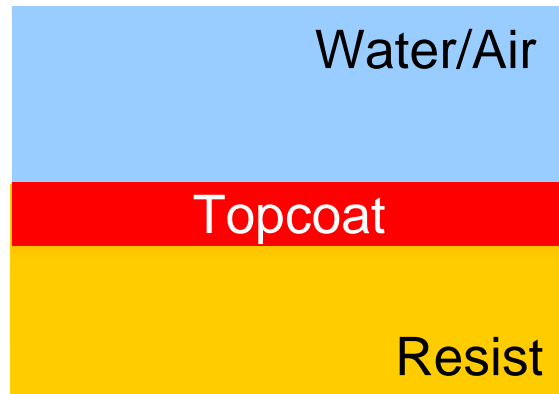
Resist

Requirements:

✓ Suppress chemical leaching

✓ Suitable scanning properties

✓ Insoluble to water, soluble to developer

✓ Excellent lithographic performance

✓ Profile compatibility to each 193nm PR

✓ No intermixing with resists

✓ No extraction from topcoats

JSR TCX topcoat series

Topcoat design

- **What knobs can we turn:**
  - Modify the acidity - dissolution rate & CA

	TC-1	TC-2	TC-3
Acidity	Higher pH	"std" pH	Lower pH
Dissolution rate	125nm/s	200nm/s	800nm/s
Residual Defects	~80,000	<100	<100
Receding Contact Angle	70	69	62
Water Mark Defects	~200	<10	~3,000

Defect reduction – TCX Topcoat

No topcoat w/ std dry resist
(ave. 10 wafers)
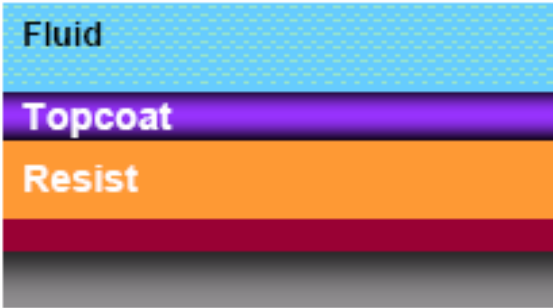
Total Defects = 122

Imm. Defects = 59

Defectivity on 0.85NA immersion scanner with & without topcoat

Legend:
- Total Defect
- Imm. Defects

Layer stack:
- TCX (90nm)
- ArF Resist (150nm)
- BARC (77nm)
- Si

Bar chart (Defect Counts):
Wafer	Imm. Defects	Total Defect
#1	6	29
#2	8	18
#3	10	27
#4	9	32
#5	12	30
#6	10	21
#7	10	42
#8	12	22
#9	9	30
#10	12	66

Without TC
Ecd 24mJ
LWR=4.1nm

With TCX
Ecd 24mJ
LWR=4.0nm
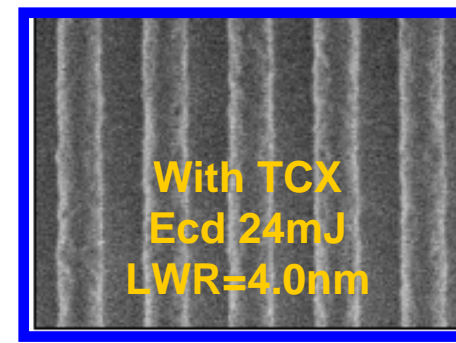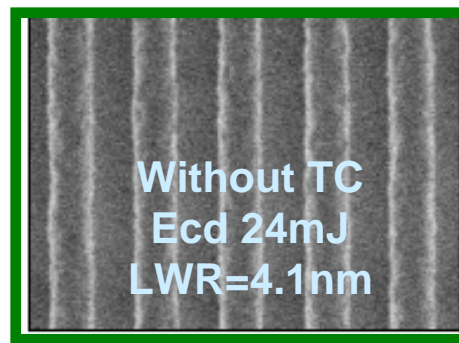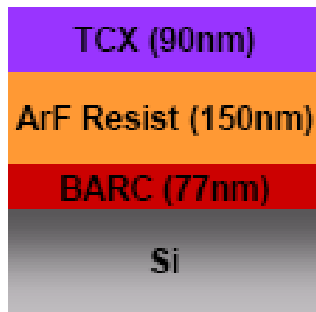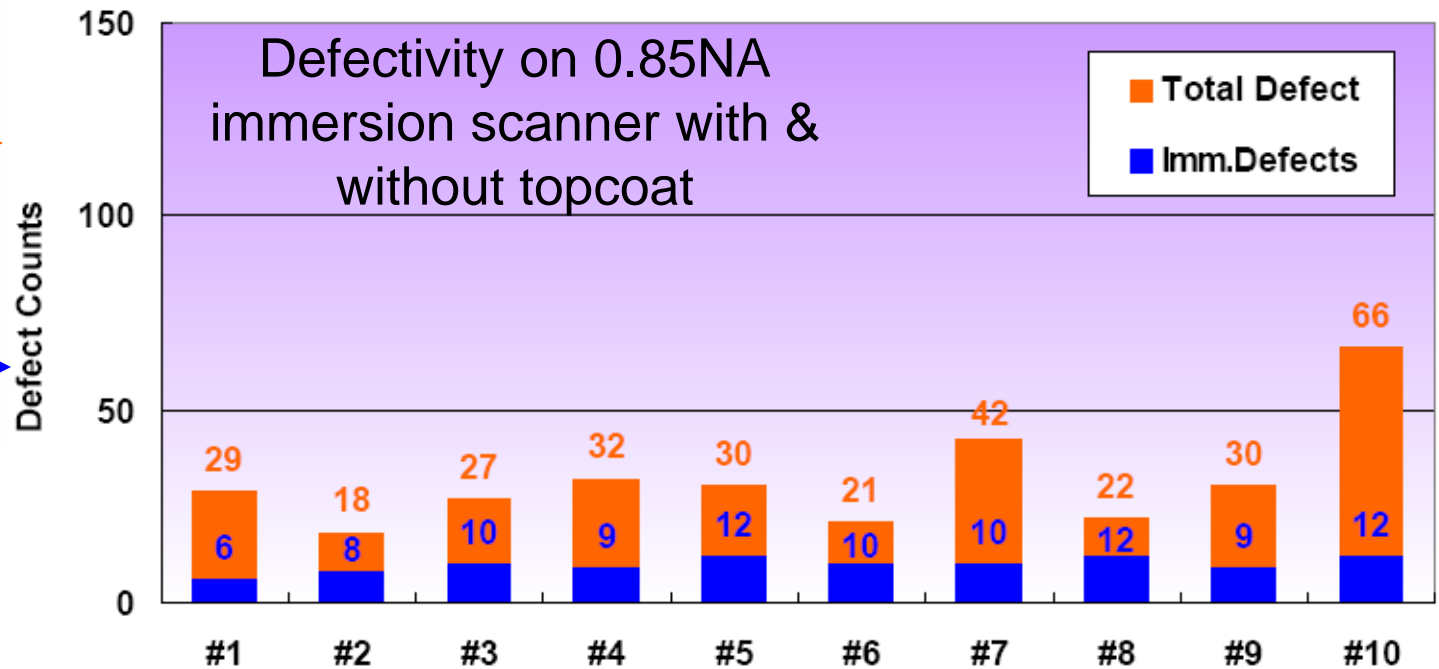
Why fix what works?
Because it's simpler! (or is it really)

Non-TC Process	TC Process
Fluid / Non-TC Resist	Fluid / Topcoat / Resist
➤ **Pro.** Enable to shorten process cycle time ➤ **Con.** Immersion specific resists, scan speed specific resists	➤ **Pro.** More reliable process for HVM at this moment, reflectivity ➤ **Con.** Additional process
Current Status Material design : Done / on-going Practical data collection : in progress High volume manufacturing : TBD	**Current Status** Material design : Done Practical data collection : Done High volume manufacturing : Done

Topcoat-less resist design

Water/Air

Topcoat
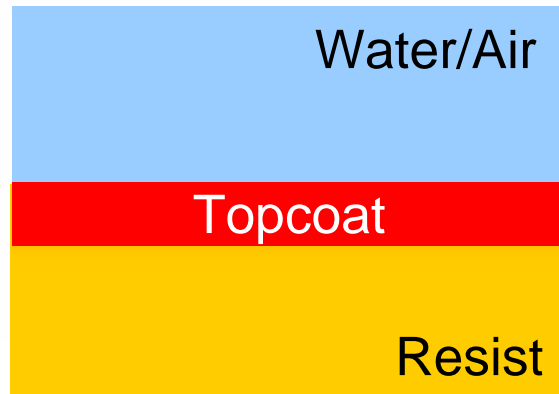
Resist

Requirements:

✓ Low chemical leaching

✓ Suitable scanning properties

✓ Balance RCA vs. ACA

✓ Excellent lithographic performance

✓ No post development defects

✓ No leaching of PAG's or other additives

✓ Try to take advantage of the maturing resist design for 193nm systems

JSR AIM resist series

What are the control knobs?

Advancing Contact Angle (ACA)

Bubble Defect

TC-less PR

Topcoats

AIM series today

Dry PR

Water Mark Defects

Physical Limitation*

Receding Contact Angle (RCA)

*** RCA < ACA**
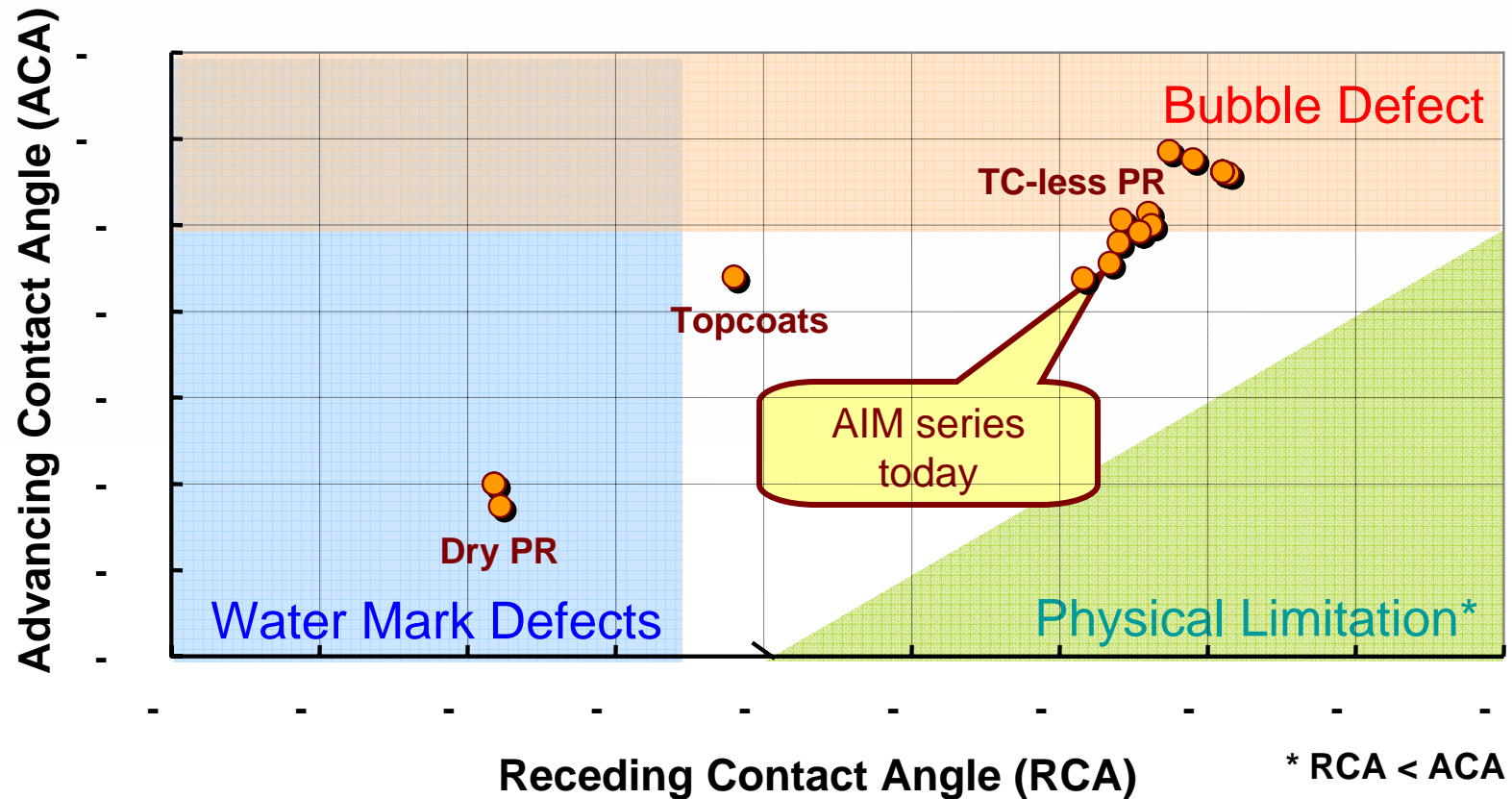
Immersion related defectivity is strongly related with RCA and ACA.

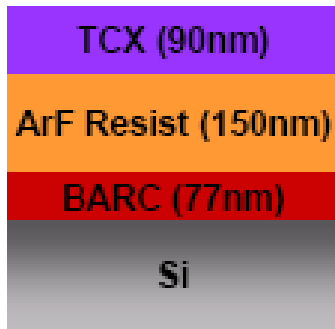# Standard resist vs. TC vs. non-TC immersion resist

	Standard	**Std. + TC**	**AIM - 1**	**AIM - 2**
Material	Dry resist	Dry resist + Topcoat	Topcoat-less resist 1	Topcoat-less resist 2
RCA	61deg.	69 deg.	86 deg.	83 deg.
ACA	80 deg.	92 deg.	98 deg.	95 deg.
Concern	RCA low Leaching & W/M	TBD	ACA high Bubble	TBD
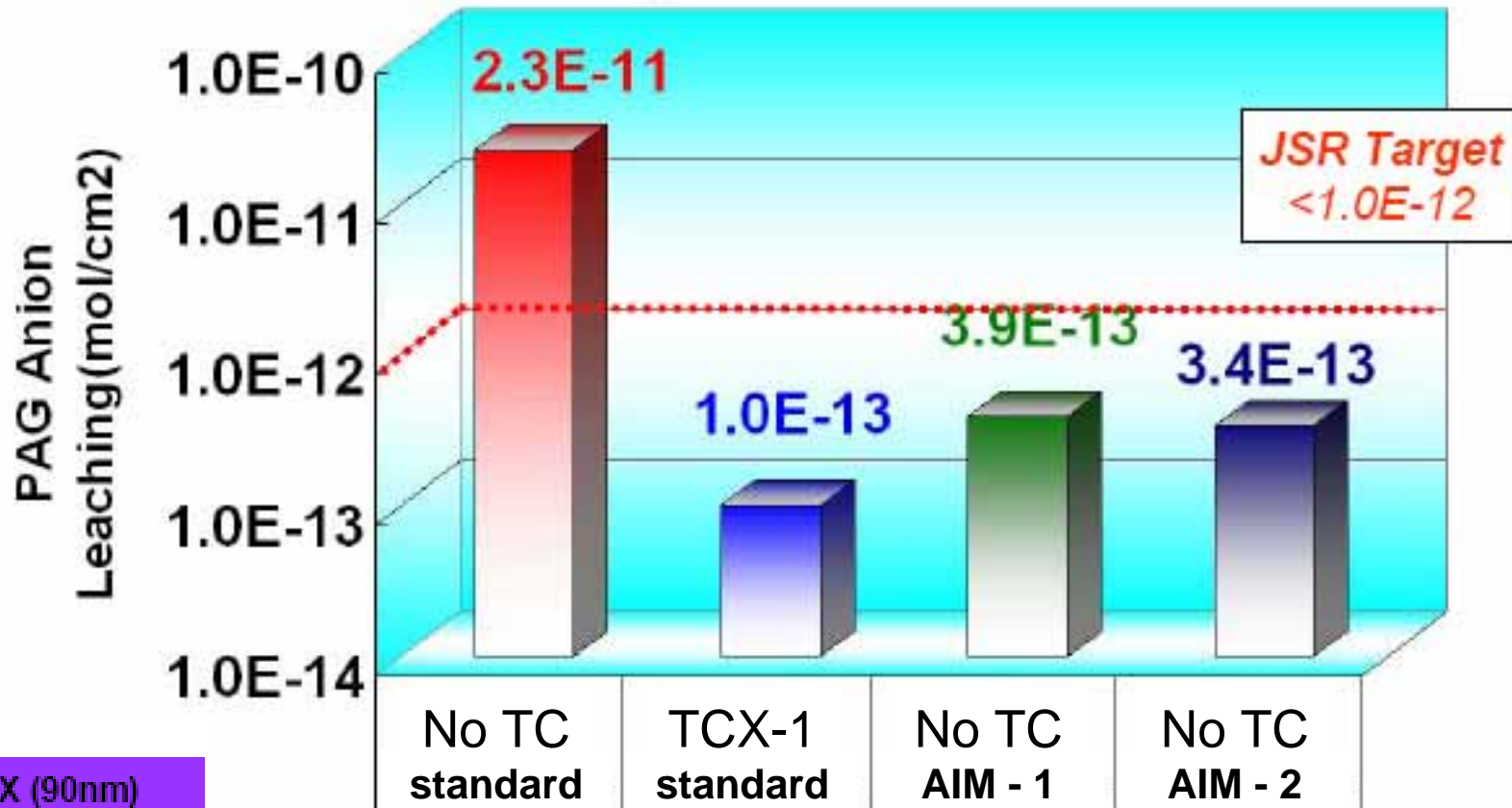
Sufficient suppression of PAG with JSR topcoat AIM resists also meet leaching specs

Std resist vs. TC vs. TC-less

Standard with TCX041
LWR:4.4nm
3σ:1.21

AIM - 1 w/o TCX041
LWR:4.3nm
3σ:1.17

AIM - 2 w/o TCX041
LWR:4.3nm
3σ:1.24
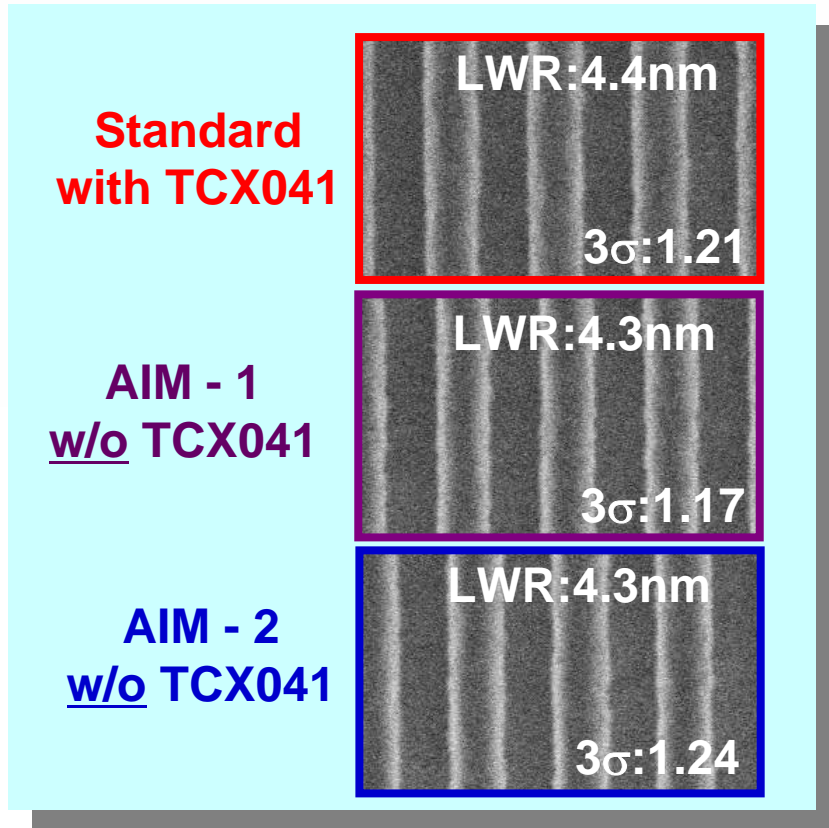
Scanner :NA=0.85, Dipole
Mask :Att-PSM(6% HT)
Pattern :65nmL/S(LF)

	Standard w/ TCX041	AIM - 1 w/o TC	AIM - 2 w/o TC
-0.35um			
-0.28um			
-0.21um			
-0.14um			
-0.07um			
BF			
+0.07um			
+0.14um			
+0.21um			
+0.28um			
+0.35um			
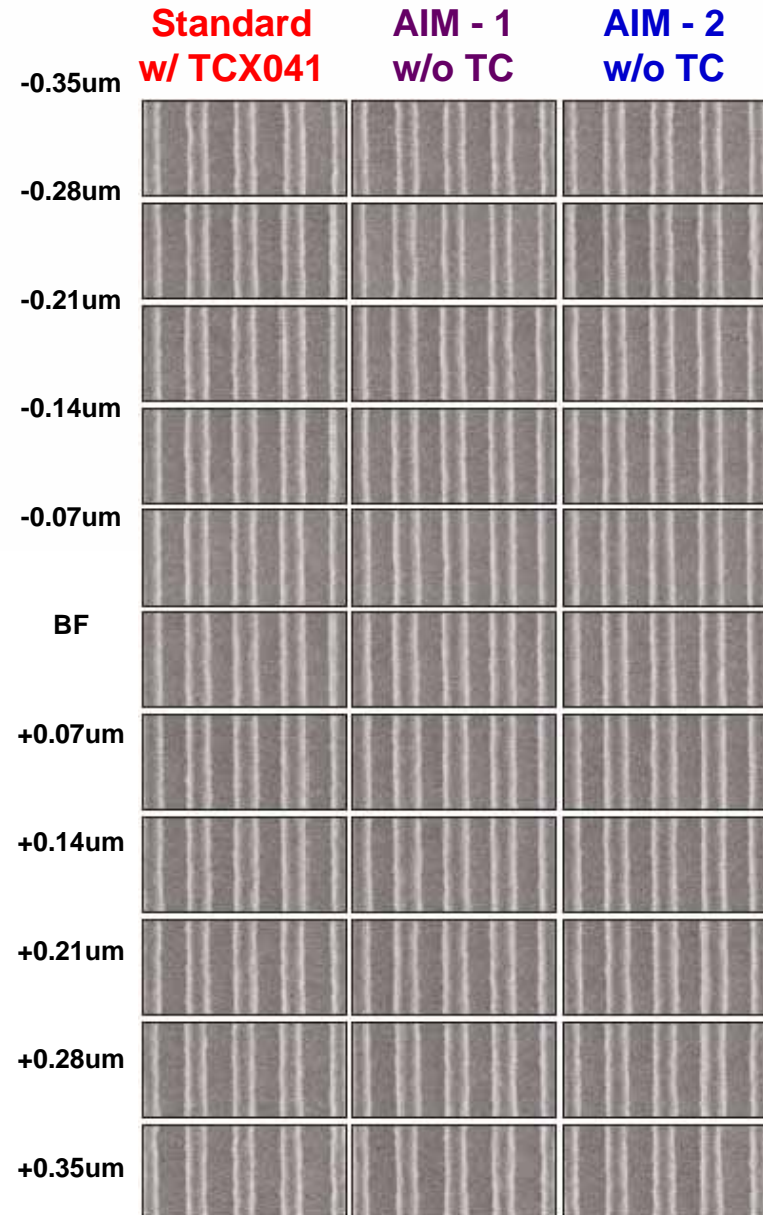
Topcoat vs. Non-Topcoat

- Optimized topcoats have been developed and proven to show HVM capability

- Understanding the RCA vs. ACA relationship is key to the success of implementing Non-TC resists

- TC vs. TC-less resists will be decided in the defectivity battlefield

- Back to our original comparison…..
  - Materials vs. the litho-cluster

The Lithocell vs. Materials

	The Lithocell	Materials
Cost	~$50,000,000	~$5000
Install time	2-4 months	2-4 hours
Foot-print	~50m^2	~500cm^2
EUV & HIL ready	Source / Lens	LWR & sensitivity / Fluids
Source of defectivity	High	Low
Who gets blamed for defectivity	Low	High
Better gifts at Semicon	iPod, etc	cookies, etc.

Total Score   2   **4**

Special Thanks

- ## JSR R&D in Japan:
  - Dr. T. Shimokawa, Y. Yamaguchi, S. Kusumoto, M. Shima, A. Soyano

- ## JSR Litho Product Development team in Sunnyvale California:
  - K. Fujiwara, J. Smith, Z. Liu

- ## Sokudo marketing team for the opportunity to present