DPT Challenges & Litho Solutions

Bob Socha
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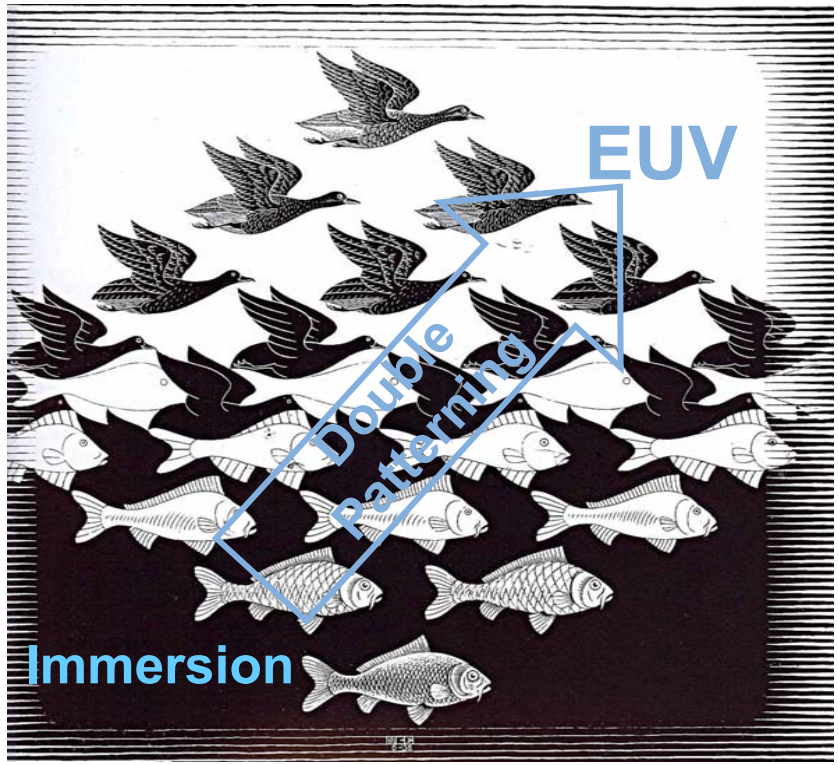

MC Escher

Outline

- SRAM gate DPT example
  - Overlay, CDU, Resolution (Design) trade-off
- Spacer Challenges
- Litho Improvements to Enable LELE & LFLE DPT
- Conclusion

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- **SRAM gate DPT example**
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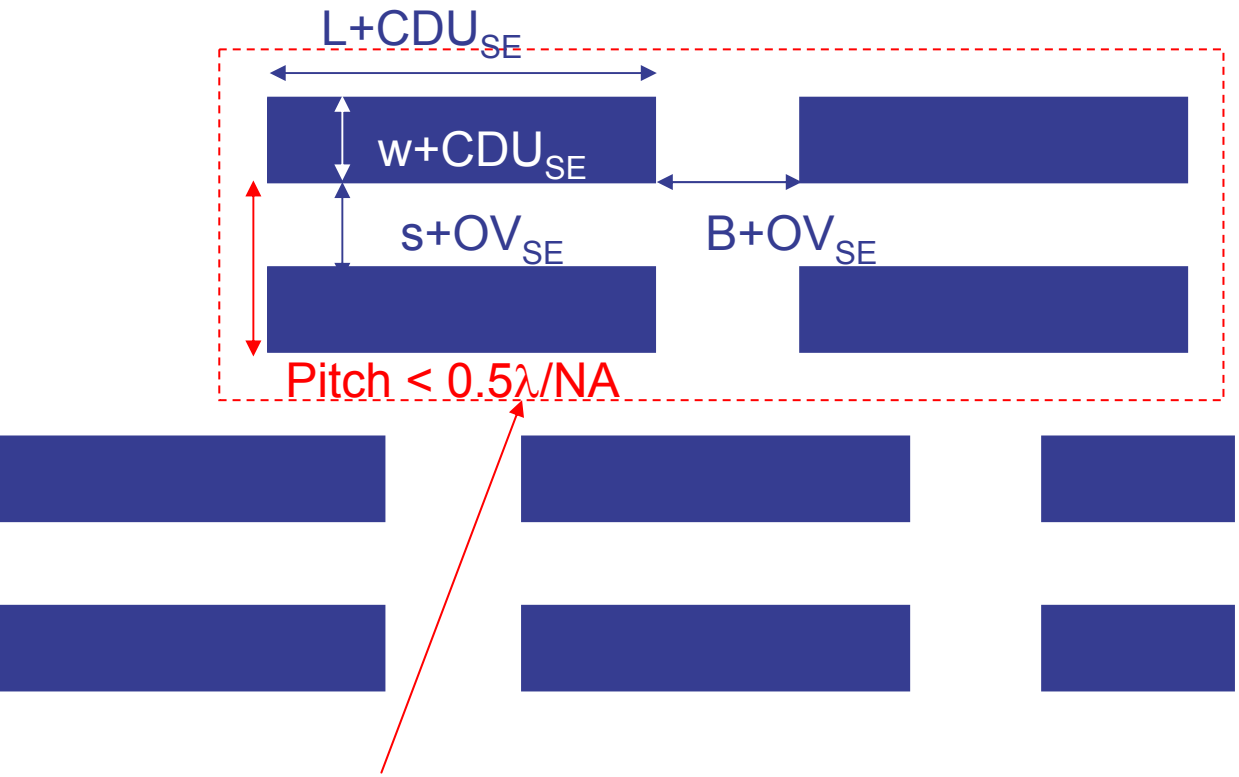
- **Litho Improvements to Enable LELE & LFLE DPT**
- **Conclusion**

Typical SRAM Gate Layer



Unit Cell needed for Area Calculation

A_{SE} is a function of 3 variables
R_{SE}, OV_{SE} and CD_{SE}

- The Area of the SRAM cell is the most widely used Metric to determine the shrink of the node
- As a result, the area must also be used to compare Litho-DPT to Spacer-DPT shrink capabilities.
  - Comparison between Litho-DPT to Spacer-DPT based on 1-D geometries (1Dmetric) is not relevant

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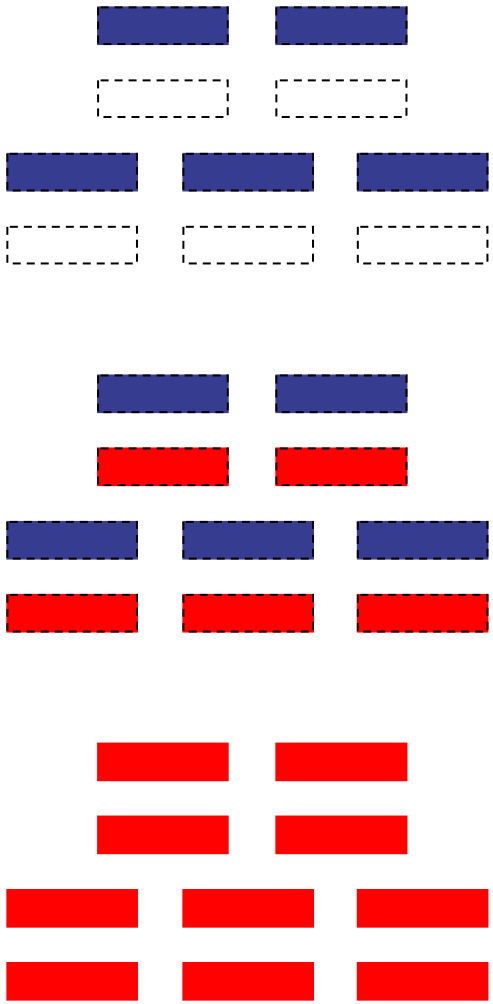
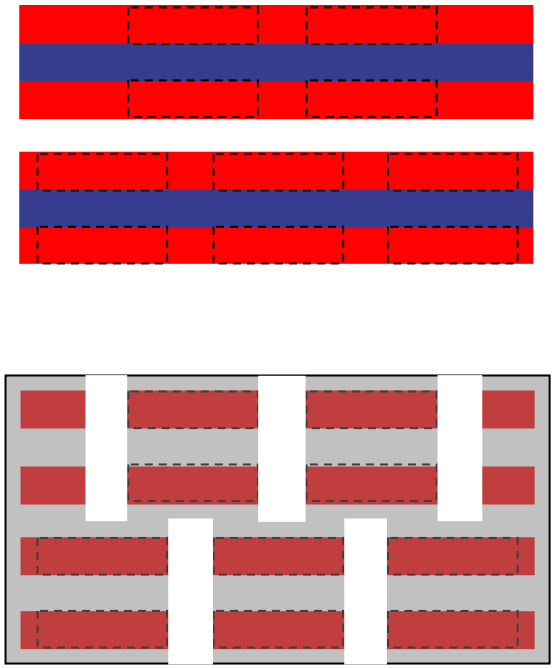
Process Steps Required

LELE



Spacer



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Double patterning require better and more lithography

Litho exposure equipment parameter as percentage of CD	Single exposure	Litho double patterning	Spacer double patterning
ΔCD	7%	3.5%	3%
Overlay (depending on DFM)	20%	7%	7-20%*
#mask steps	1	2	2-3
# process steps relative to single exposure	1	2	3-4
Application	2D, All	2D, All	1D, Mainly Memory

* Depending on the amount of “Design For Manufacturing” effort

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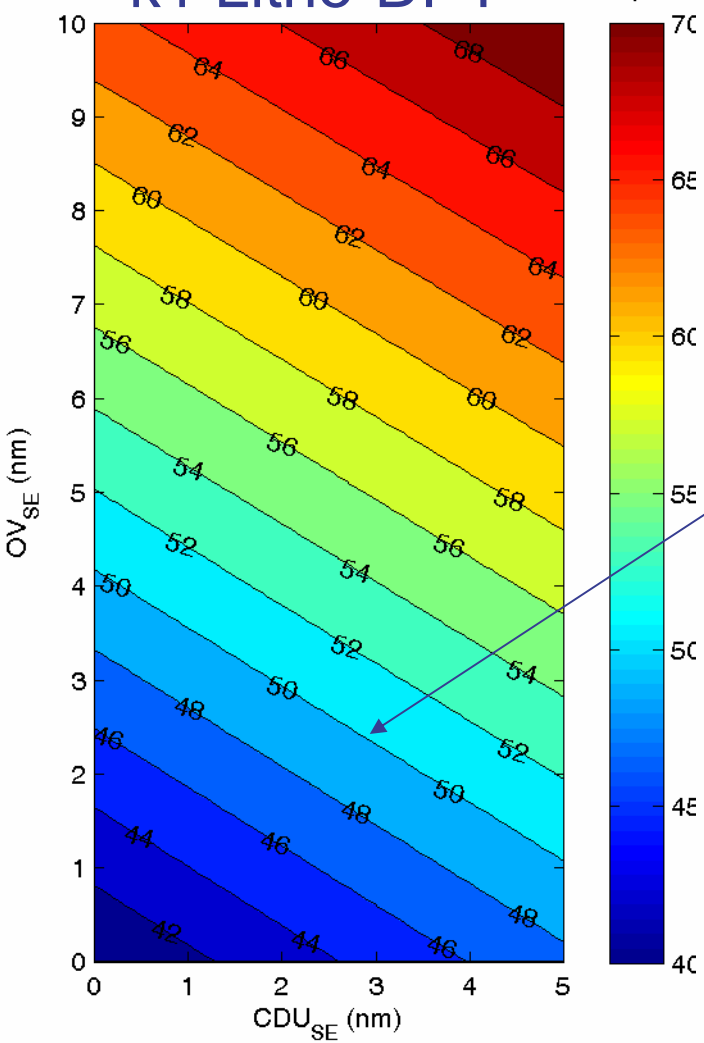
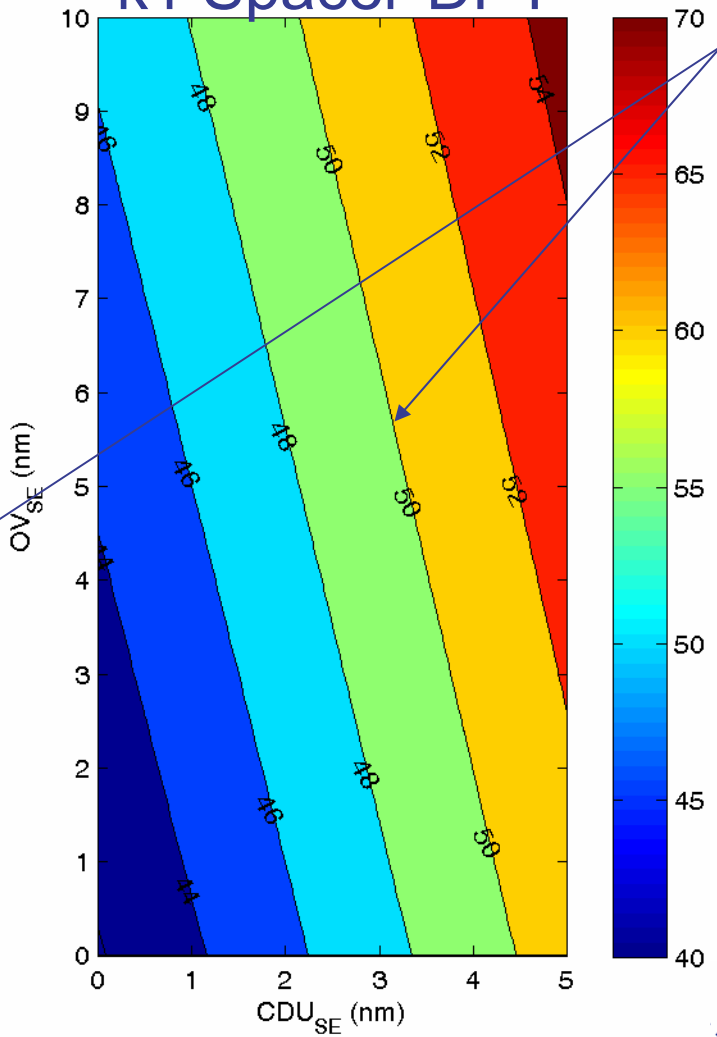
OVSE and CDUSE requirements for 35nm HP SRAM (shrink of the 50nm HP SE SRAM area by 50%)

k1 Litho-DPT



k1 Spacer-DPT



- Below 50% line is the area of interest
- OV_{SE} must be less than 2.5nm for 50% shrink with Litho-DPT at CDU_{SE}=3nm
- If current CDU_{SE}=3nm and OV_{SE}=5nm, a 56.2% shrink can be done with Litho-DPT
- If current CDU_{SE}=3nm and OV_{SE}=5nm, a 49.5% shrink can be done with Spacer-DPT

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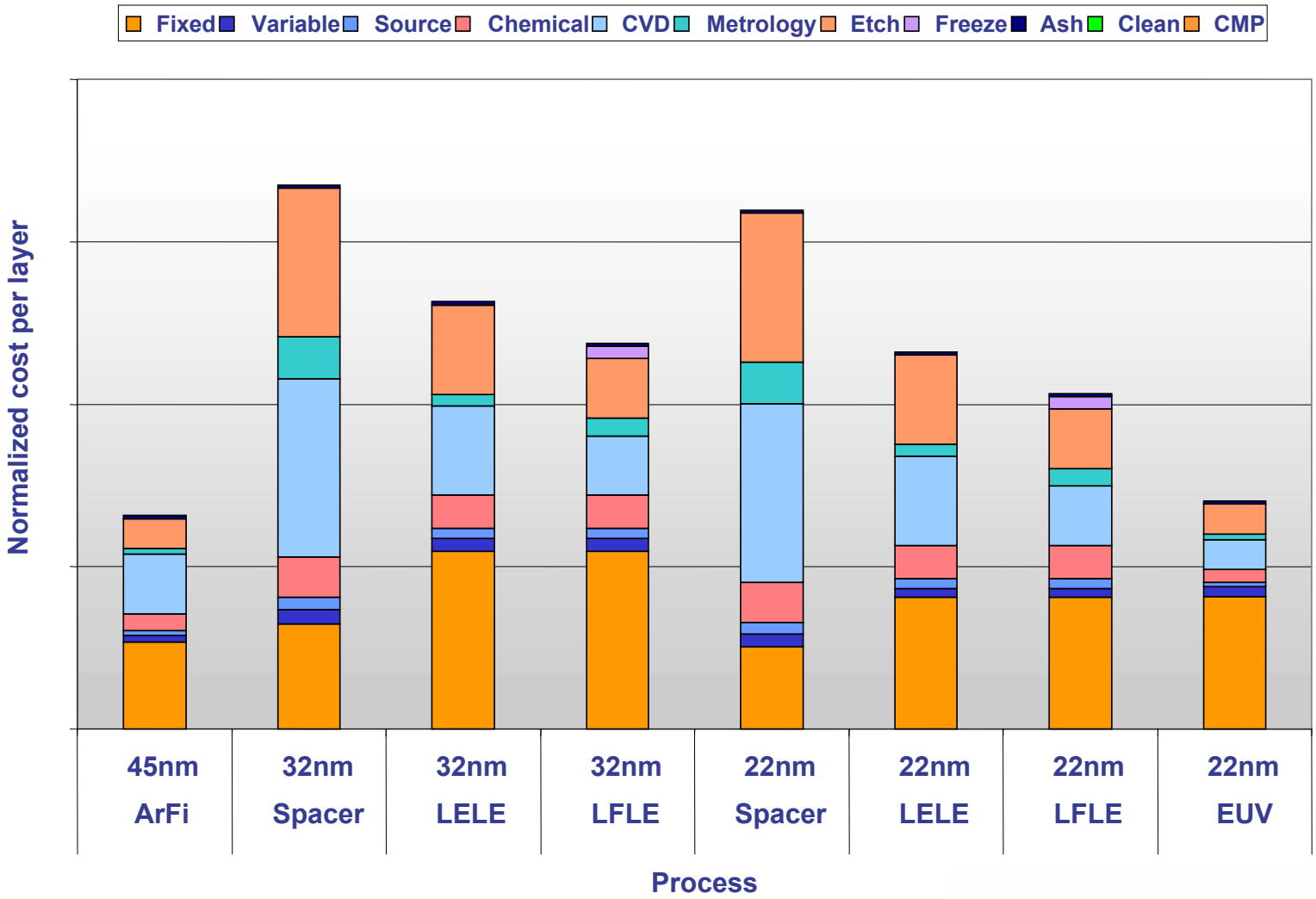
Litho cost per layer: estimates for 32 nm & 22 nm

Single exposure schemes more cost effective



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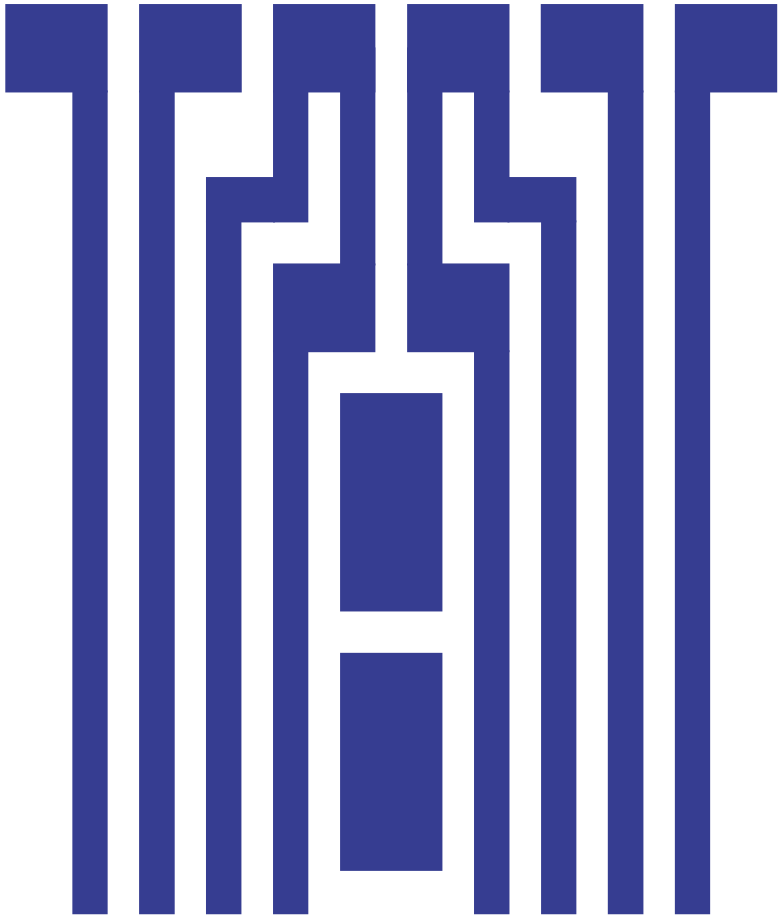
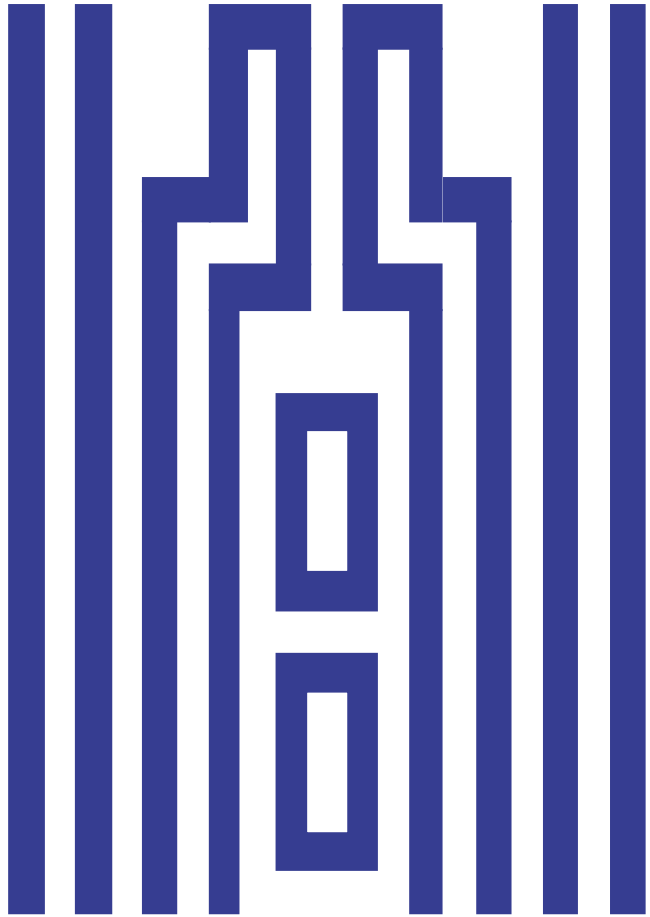
Spacer process can be used for random structures

Desired layout



After spacer process applied



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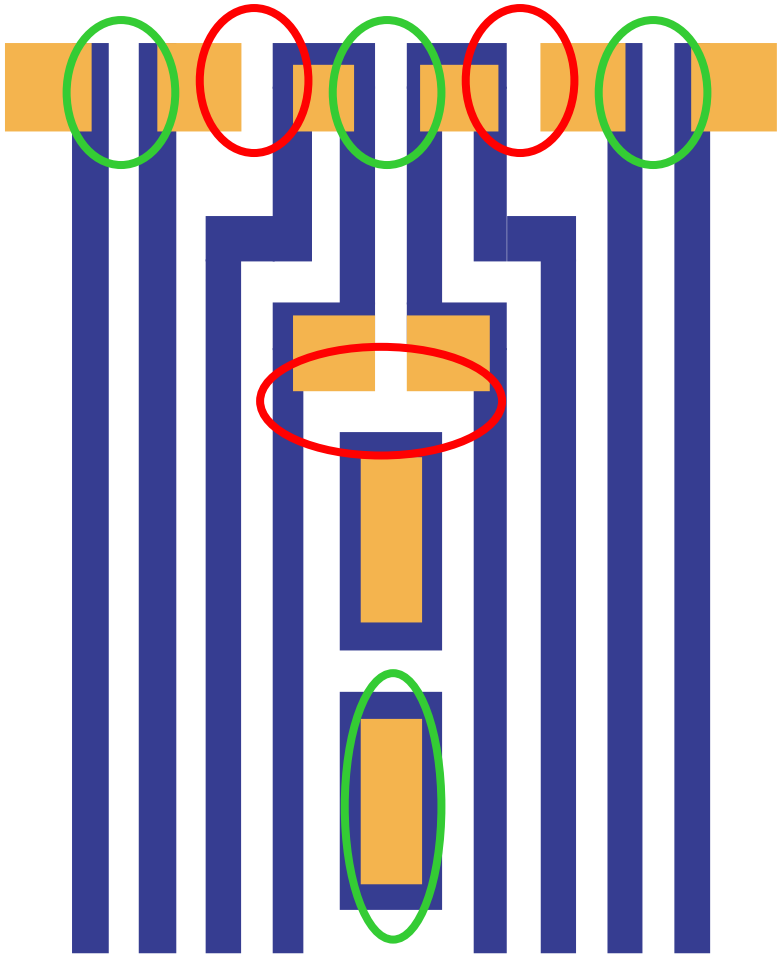
Spacer needs overlay friendly layout

to enjoy overlay advantage from the self aligned process



- Areas surrounded by geometry formed by spacer are less sensitive to overlay errors.
- Areas not surrounded by geometry formed by spacer are more sensitive to overlay errors. Possible CD error or bridging can occur.
- Without design change, overlay is still critical for spacer when exposing a clear field mask!

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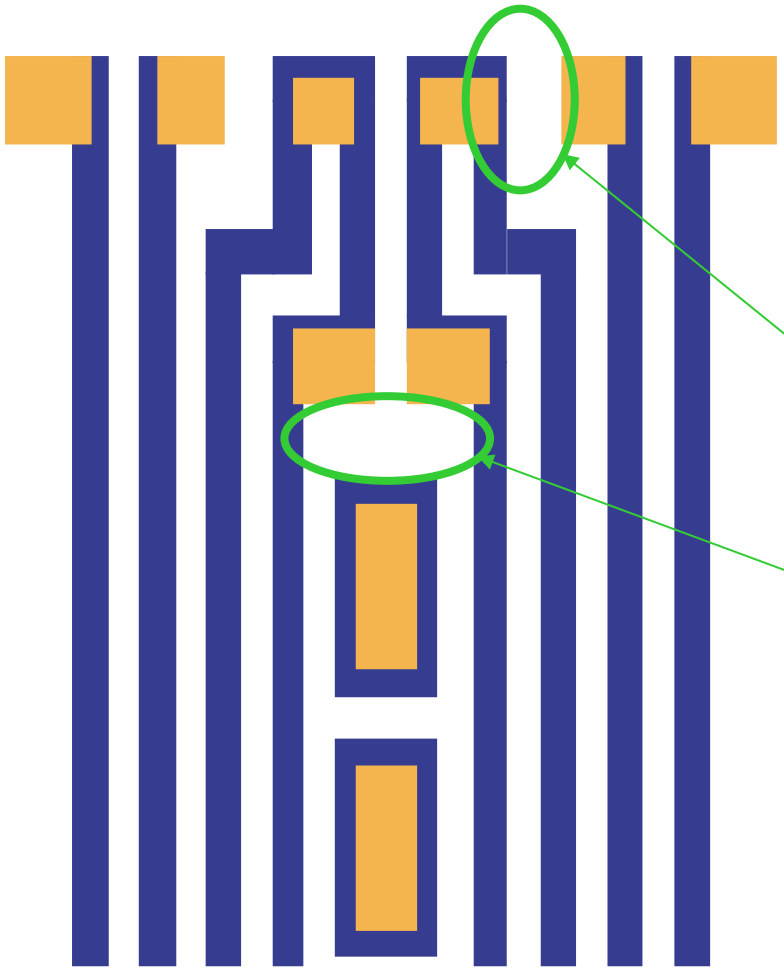
Spacer with overlay friendly layout

to enjoy overlay advantage from the self aligned process



- In areas not surrounded by geometry formed by spacer, the space width between patterns must increase.
- Design change to increase the space width between patterns may need tighter overlay for next layer.
- Design change to shift a pattern to increase space width may require verification of the electrical performance.
- With these design changes, the cell size may increase.

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Spacer Challenges

- **CoO is higher with Spacer DPT compared to LELE/LFLE DPT**
  - **Spacer process integration/complexity increases cycle time**
- **Not all designs can benefit from Spacer DPT self-alignment**
  - **Burdens the designer or makes design rules overly restrictive**
  - **Industry not yet ready for Spacer friendly designs**
- **How can litho improvements mitigate the Spacer Challenges?**

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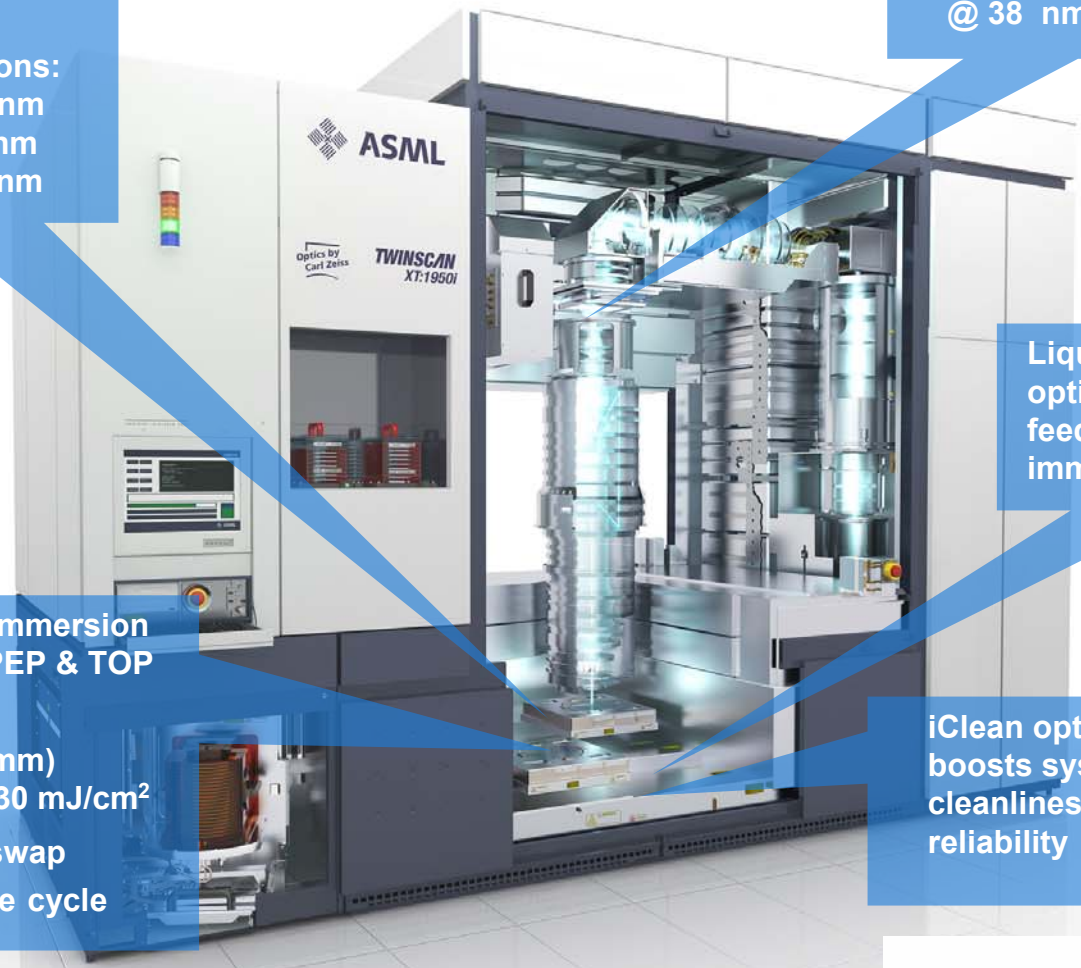
TWINSCAN™ XT:1950Hi

Improved overlay performance options:
DCO ≤ 3.5 nm
SMO ≤ 4.0 nm
MMO ≤ 7.0 nm

Advanced lens control means improved imaging performance @ 38 nm resolution



Liquid particle counter option gives fast feedback and control of immersion water quality

Best-in-class immersion productivity (PEP & TOP options):

148 wph (300 mm)
125 x 16x32 x 30 mJ/cm^2

Faster chuck swap

Faster measure cycle

iClean option boosts system cleanliness and reliability

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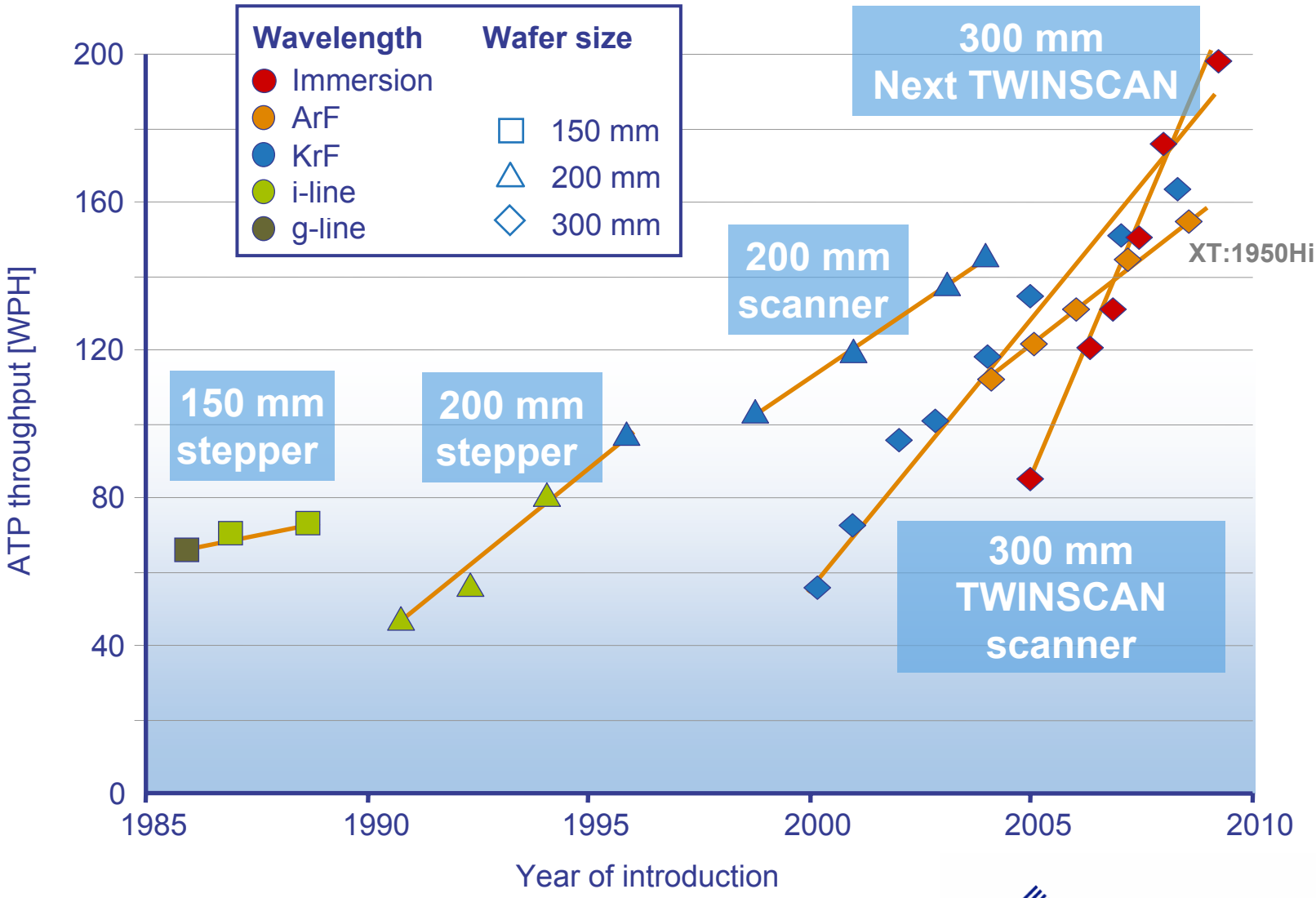
ASML system throughput improvement drives CoO



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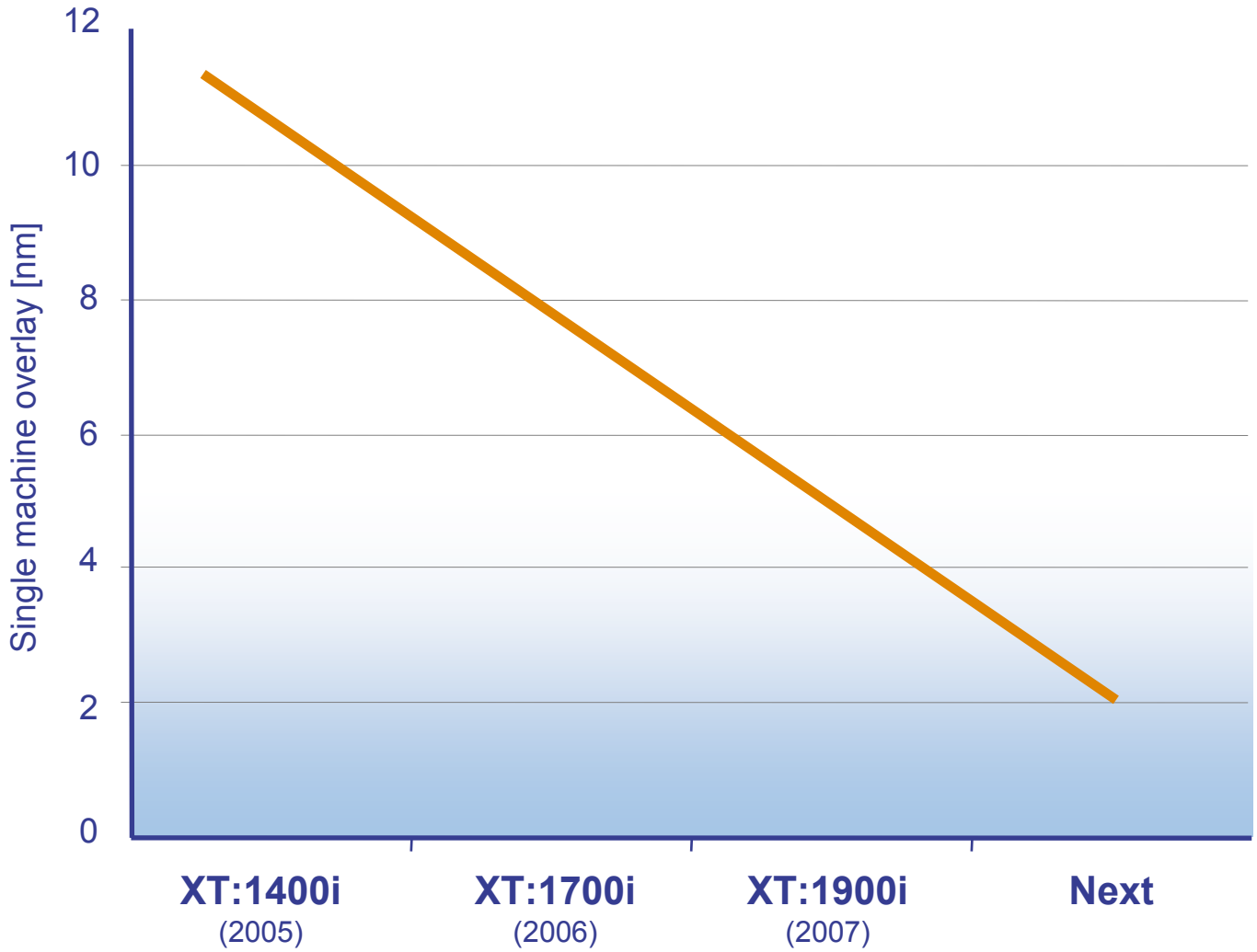
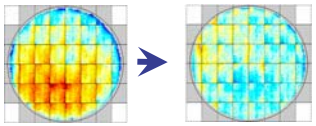
TWINSCAN immersion overlay trend

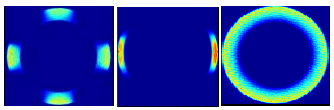


ASML mask and system enhancements extend lithography to the limit of k_1

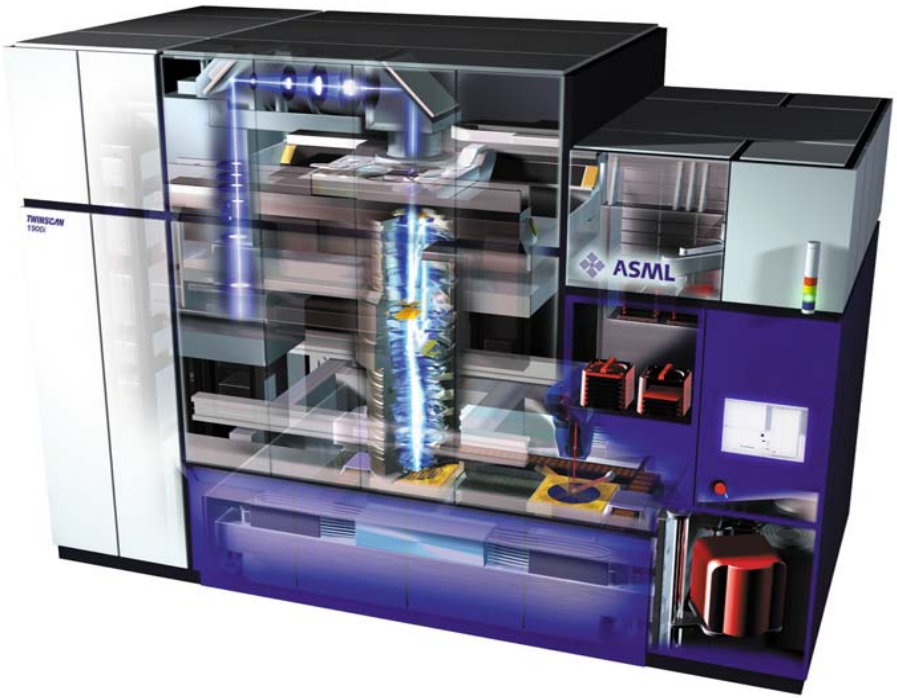


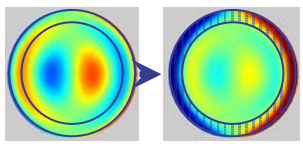
DoseMapper for optimum CD Uniformity

GridMapper for improved Overlay

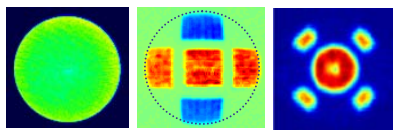


Flexible off-axis & polarized illumination

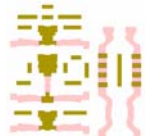




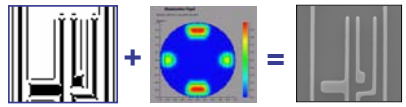
Application specific lens setup



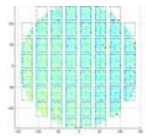
In-built wave-front, polarization and pupil metrology



Mask enhancement techniques & optimization software



Illumination source optimization & software



Offline Dual stage wafer height mapping
Focus Dry, Expose Wet

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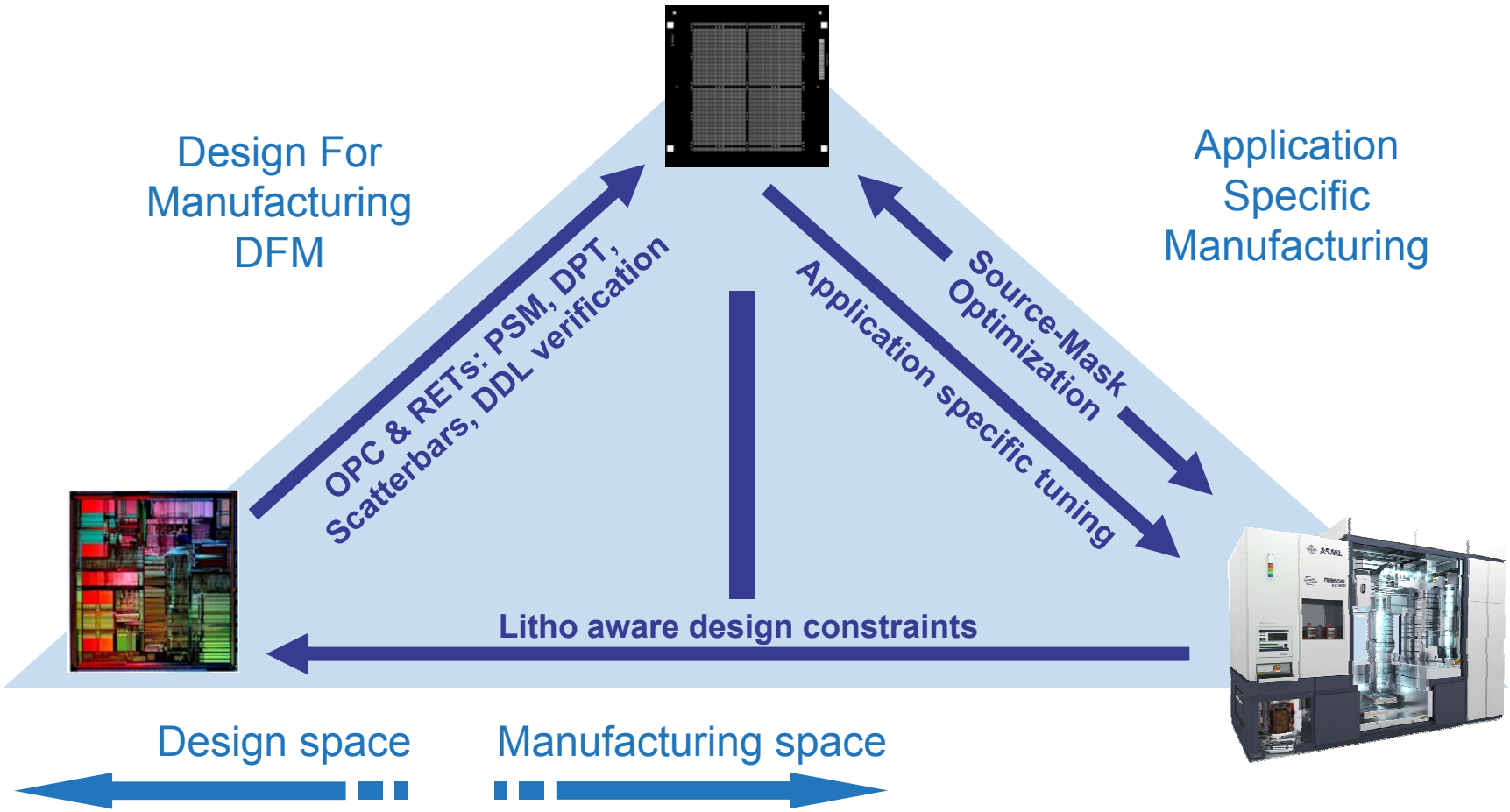
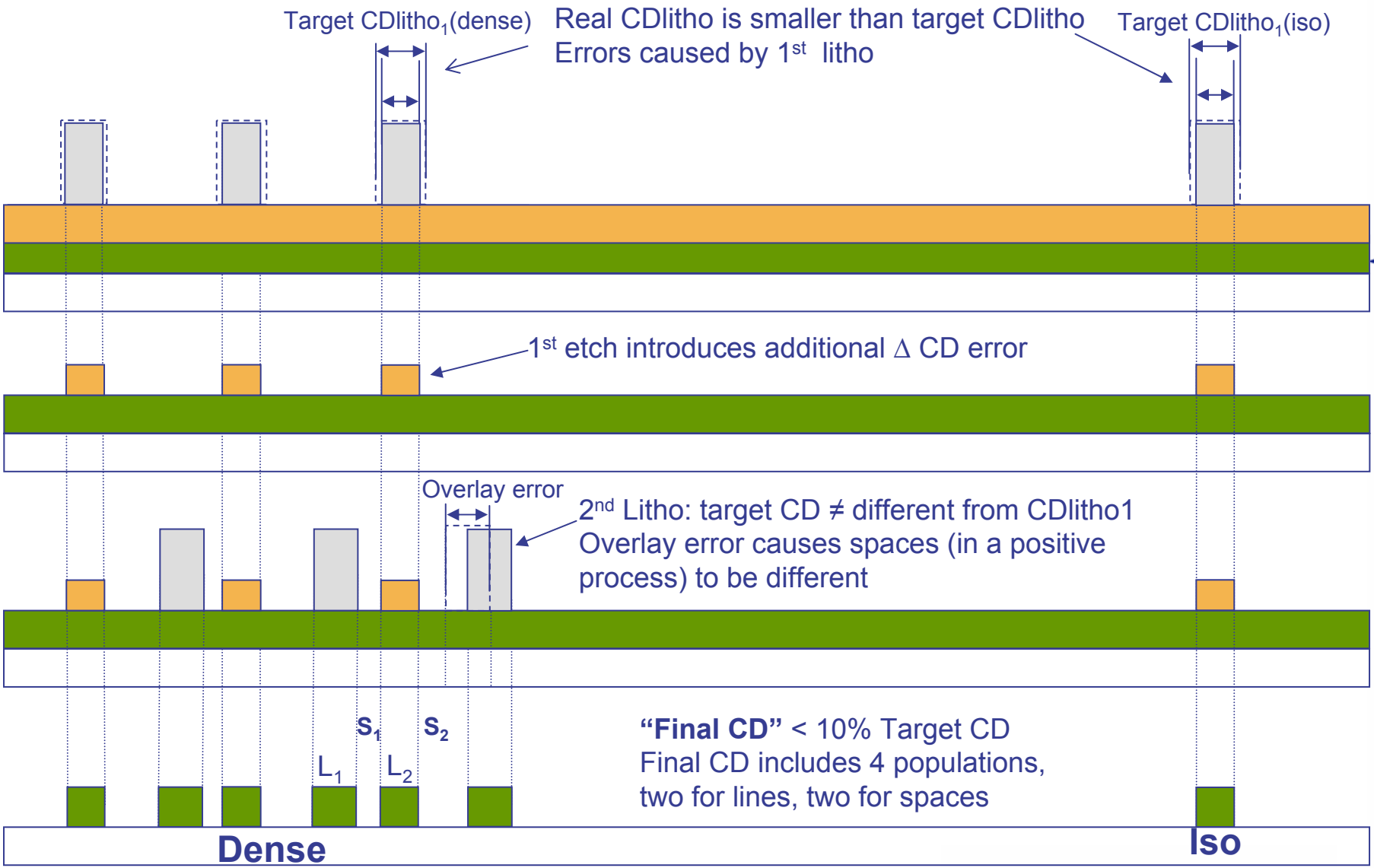
Low k_1: High design to wafer integration

Low k_1 (<0.4): Integration of design, mask and lithography processes



LELE: CDU for Isolated and Dense Lines



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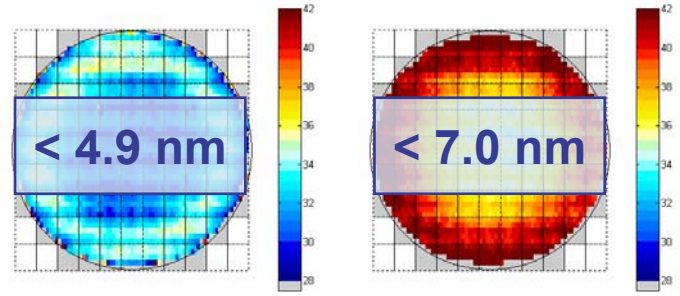
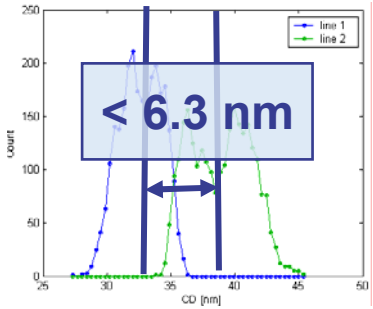
Litho patterning process control for CD and Overlay of 32 nm, using angle-resolved scatterometry

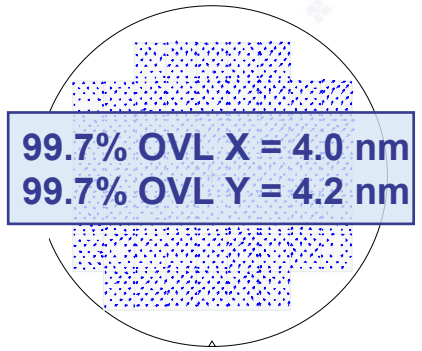
Raw etched poly CDU



Mean CD



Overlay between litho 1 and 2

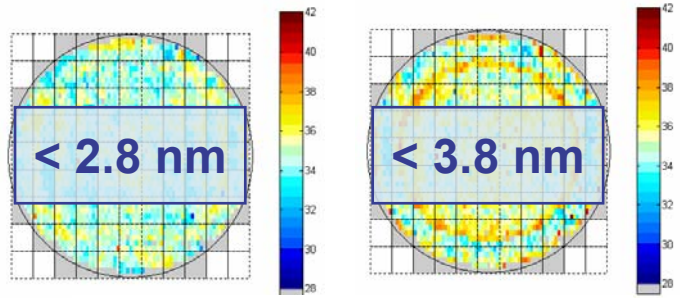


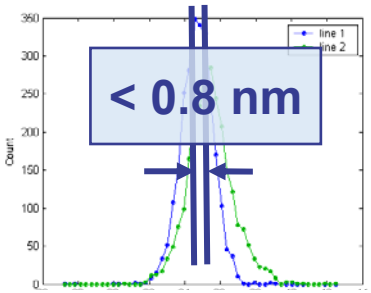
Line1 Line2

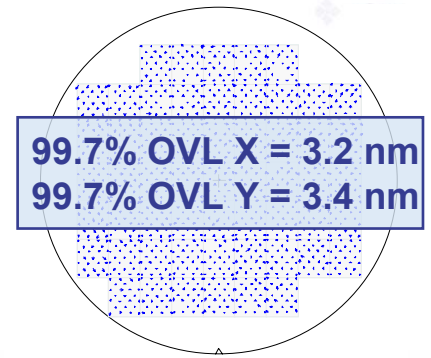
DoseMapper recipe

DoseMapper recipe

Optimum GridMapper recipe







DoseMapper corrected etched poly CDU

mean CD

 Jo Finders et al. | SPIE San Jose, Feb 26, Ref. 6924-07
"Double patterning for 32 nm and below, an update".

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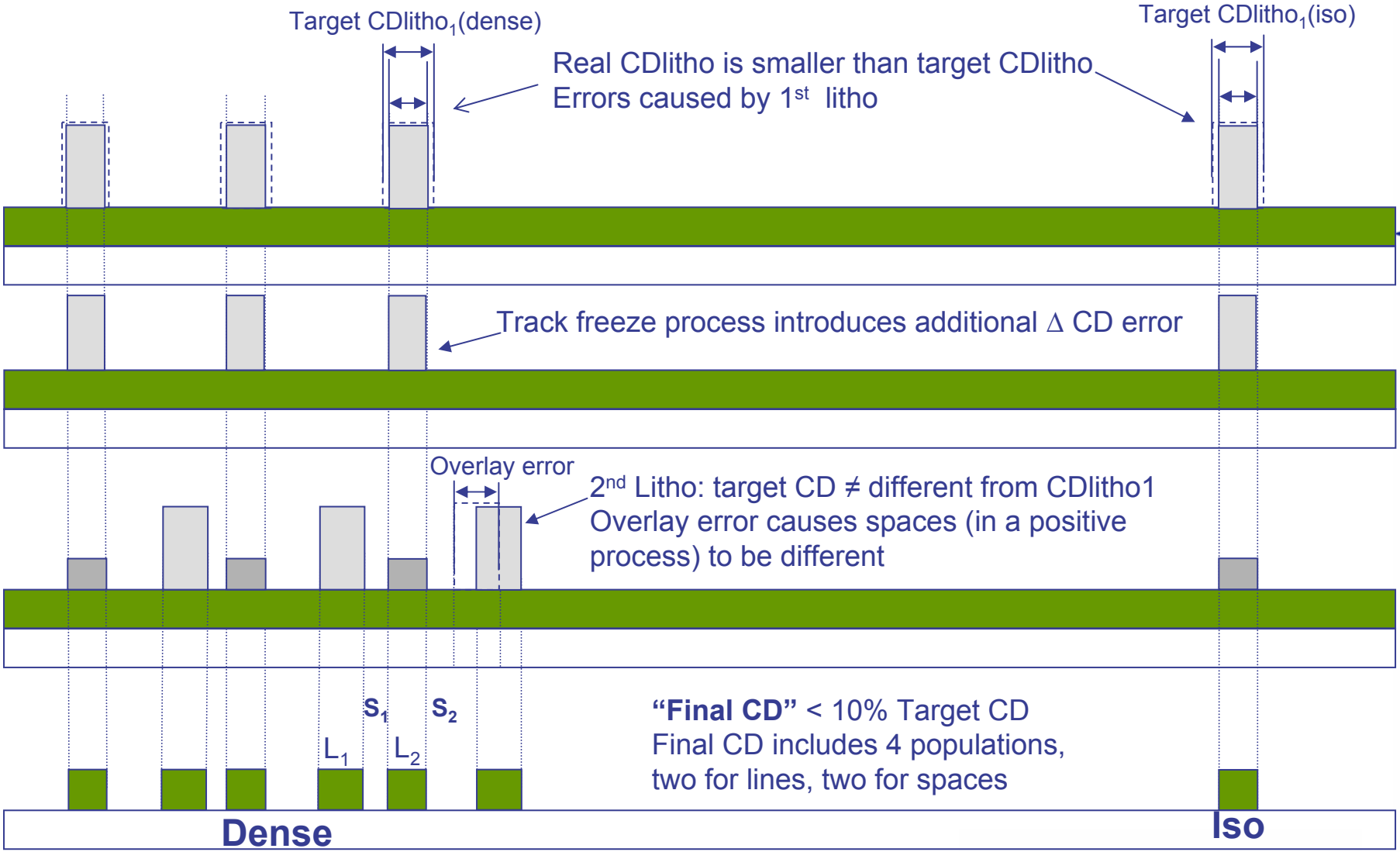
LFLE: CDU for Isolated and Dense Lines

Wafer does not leave litho cluster



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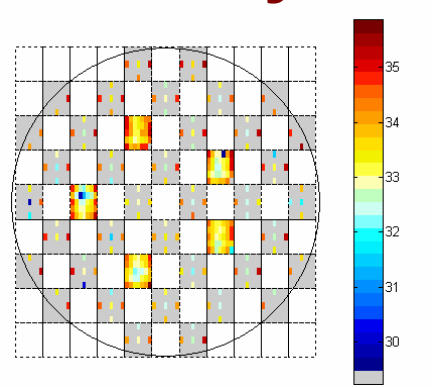
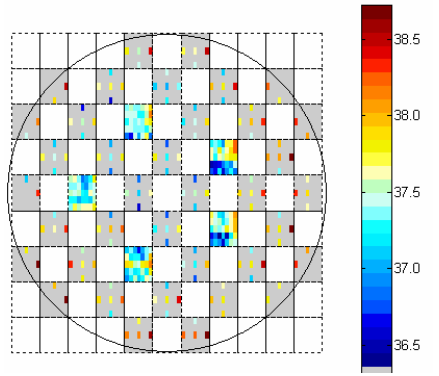
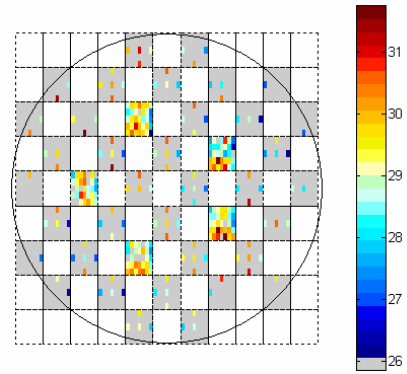
Litho double patterning process (LFLE) control for CD & Overlay of 32 nm: wafer did not leave the litho cell



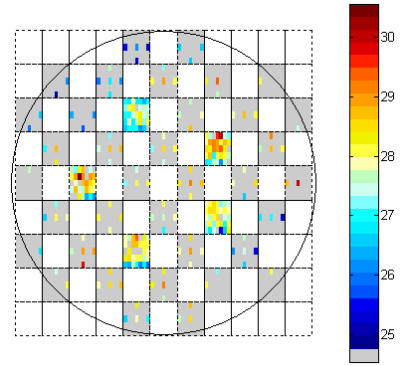
Line1
Mean=33.5
3σ=2.8nm



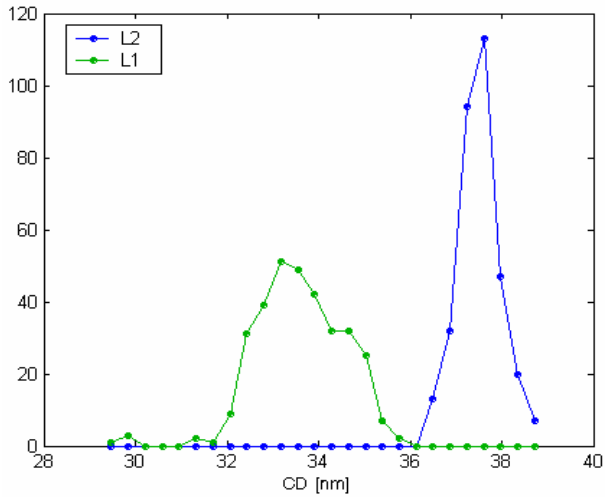
Line2
Mean=37.5
3σ=1.3nm



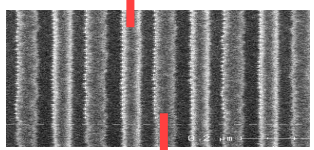
space1
Mean=29.1
3σ=3.3nm



space2
Mean=27.8
3σ=2.7nm

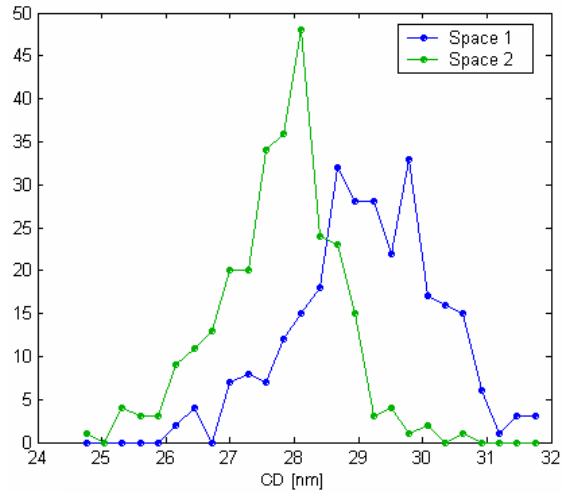


Litho 1



Litho 2

NA=1.0
Dipole illumination
σ_0/σ_i=0.86/0.65



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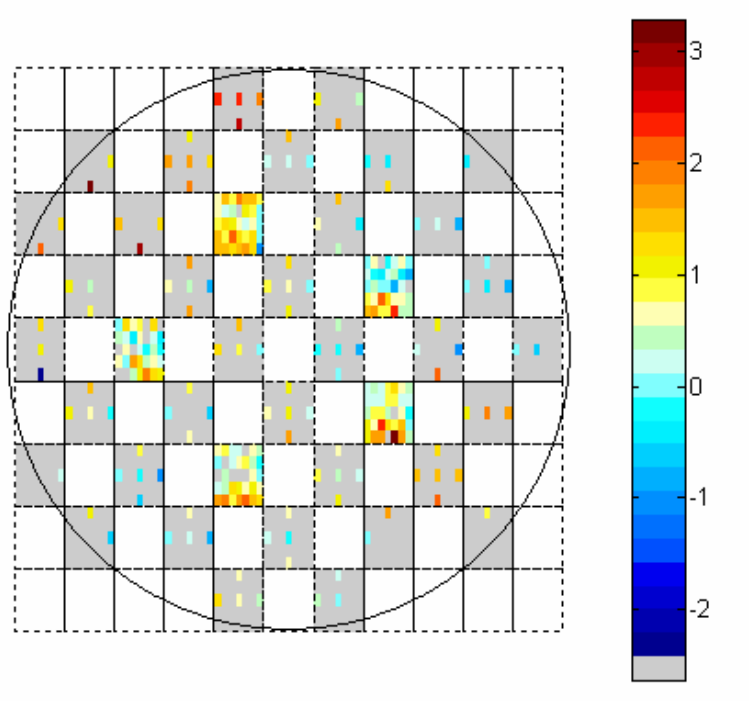
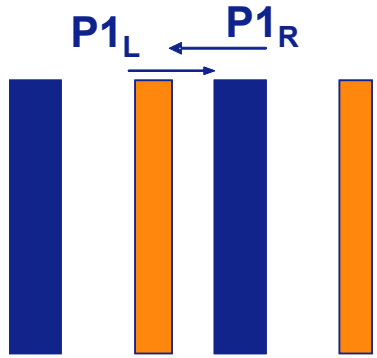
Litho double patterning process (LFLE) control for CD & Overlay of 32 nm: wafer did not leave the litho cell





$$DPT\_OL = P - P_1 \qquad P_1 = \frac{P_{1L} + P_{1R}}{2}$$

Overlay

x

Mean:	0.71
3 Sigma:	2.38
Max:	3.29
99.7%:	3.19
Nr. of points:	331
Nr. of flyers:	53

DPT overlay 3σ<2.5nm

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Conclusions

- Spacer Challenges
  - Not all designs can benefit from Spacer DPT self-alignment
  - Burdens the designer or makes design rules overly restrictive
  - Additional cost/complexity (cycle time) serves as a detractor
- Litho Challenges/Improvements
  - Spacer, LELE & LFLE require much tighter CDU than required from SE lithography; LELE/LFLE must also achieve overlay on the order 3nm
  - Intra-layer overlay not as challenging as inter-layer overlay due to elimination of some process effects.
  - Tighter CDU and overlay budgets should be achieved through active compensation of wafer and field spatial distributions
  - DoseMapper to reduce intra-field and inter-field CDU due to reticle, track, and etch CD variation
  - GridMapper to reduce intra-field and inter-field OV due to reticle registration and wafer distortion
- XT:1950Hi drives performance improvements to further enable DPT processing.
- Future improvements planned in productivity, overlay & imaging to enable cost effective lowk1 solutions.

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Acknowledgement

- **ASML**
  - **Donis Flagello, Jo Finders, Mircea Dusa, Skip Miller, David Deckers, Ad Lammers, Dorothe Oorschot, Bart Rijpers, Paul de Haas, Christian Leewis, Martyn Coogans, Eddy van der Heijden, John Quaedackers, Jeroen Meessen, Toine de Kort, Joris Kuin, Robert Routh,** Andre Engelen, Eelco van Setten, Mark van de Kerkhof, Hans Bakker, Jos de Klerk, **Koen van Ingen Schneau, Noreen Harned**
- **IMEC**
  - Mireille Maenhoudt, Shaunee Cheng, Patrick Jaenen, Tom Vandeweyer, Diziana Vangoidsenhoven
- **Carl Zeiss**
  - **Winfried Kaiser,**

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Commitment
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