Cost effective scaling: next-generation lithography progress and prospects

Sokudo Breakfast Forum
Semicon West

July 10th, 2013

Skip Miller
Outline

• Why EUV & 450mm

• Roadmap & scanner status
  • Roadmap
  • EUV performance status
  • 450mm status

• Summary
Moore’s law: *Doubling of components per chip every 12 months resulting in a lower cost per component*

"Cramming more components onto integrated circuits“, *Electronics Magazine* April 19, 1965
Moore’s Law: what it means for consumers

Source: Gartner. High quality Flash
IC manufacturers’ roadmaps support further device scaling

2012 - 2013

- **22 - 20nm node**
  - Memory: 0.09um2, SRAM
  - Device: planar or FinFET (Intel)
  - Gate: RMG-HKMG
  - Channel: Si
  - Vdd: 0.8V

2014 - 2015

- **16 - 14nm node**
  - Memory: 0.08um2 SRAM
  - Device: FinFET, FDSOI
  - Gate: RMG-HKMG
  - Channel: Si; (Si)Ge
  - Vdd: 0.6V

2016 - 2017

- **11 - 10nm node**
  - Memory: 0.06um2 SRAM
  - Device: FinFET
  - Gate: HKMG
  - Channel: Si, Ge, IIIVr
  - Vdd: 0.5V

2018 - 2019

- **8 - 7nm node**
  - Memory: FBRAM, STT-RAM, >8T SRAM
  - Device: FinFET, Nanowire, TFET
  - Gate: HKMG
  - Channel: IIIV-Graphene

38 - 32nm node

- Memory: stacked MIM
- Peri: planar
- Array: 6F2, bWL
- Gate: poly/SiO2
- Channel: Si
- Vdd=1.35V

29 - 22nm node

- Memory: stacked MIM
- Peri: planar HKMG
- Array: 6F2, bWL
- Gate: HKMG
- Channel: Si
- Vdd=1.2V

22 - 16nm node

- Memory: stacked MIM
- Peri: planar
- Array: 6F2, 4F2, bBL, LBL, 1T1C(VFET)
- Gate: HKMG
- Channel: Si
- Vdd=1.1V

16 - 14nm node

- Memory: FBRAM, STT-MRAM, RRAM, PCRAM
- Peri: planar
- Array: 4F2, 1T, 1T1R, 1T1MTJ(VFET)
- Gate: HKMG
- Channel: Si
- Vdd≈1V

19 - 16nm hp

- 4.5F - 6F2 asymmetric cell
- Density: 128G
- Device: FG

16 - 13nm hp

- 3D NAND intro at 5x → 4xmn
  - 6F2 asymmetric cell
  - 4F2 symmetric cell
  - Density: 256-512G
  - Device: dual-FG

~ 11nm hp (planar)

- 3D NAND at 3x → 2xnm X-pt intro at 2xmn
  - 7F2 asymmetric cell
  - 4F2 symmetric cell
  - Density: 512-1024G
  - Device:: dual-FG, BiCS in HVM(@4xmn)

< 10nm hp (planar)

- X-pt intro at 2xmn
- Density: > 1T with 3D chip stacking
- Device: 3D BiCS, XPoint-RRAM
- Selector: diode

Source: IMEC, ASML TDC, Jan 2013
Industry roadmap towards <10 nm resolution

Lithography roadmap supports continued shrink

- NAND 17%
- DRAM 13.9%
- Logic 14.1%

Resolution / half pitch, "Shrink" [nm]

- AT:1200
- XT:1400
- XT:1700i
- XT:1900i
- XT:1950i
- NXT:1960Bi
- NXE:3100
- NXE:3300B
- NXE:3350B
- NXE:3400
- NXE:3350B
- NXT:1970Ci

Year of Production start *

- Feb-2013

LE = Litho-Etch, n = number of iterations

SADP = Self Aligned Double Patterning

SAQP = Self Aligned Quadruple Patterning

* Note: Process development 1.5 ~ 2 years in advance

Single Exposure

2D LE^n Patterning

1D SADP

1D SAQP

DUV

EUV

Public Slide 6

Feb-2013
Cost becomes a concern post 28 nm

Sources:
- nVidea, ITPC, nov, 2011
- Broadcom, IMEC, may 2012
- GF, ISS, jan 2013
Litho roadmap supports cost per gate roadmap
EUV needed to enable industry target

Industry target: Cost/gate 70% node over node

Source: ASML
Litho roadmap supports cost per gate roadmap
EUV needed to enable industry target

Performance enhancement planned on the 20 nm design rule through finFET or SOI

Source: ASML
Only EUV can enable 50% scaling for the 10 nm node
Layout restrictions and litho performance limit shrink to ~25% using immersion

Source: ARM, Scaled N20 nm flip-flop design
Even gridded SRAM designs prefer EUV at 10 nm

Limited overlay between local interconnect layers makes multiple patterning very difficult

Quadruple expose immersion

1) Small overlapping process window
2) Marginal CD control
3) Failing overlap at 3 nm overlap

All exposures have to match to each other to enable sufficient Metal 1 to 2 overlap, leading to tight overlay requirements
Even gridded SRAM designs prefer EUV at 10 nm
Limited overlay between local interconnect layers makes multiple patterning very difficult

Integrated transistor performance on EUV superior compared to ArF double patterning

Cumulative probability actual transistor performance < Idp %

Saturated drain current, Idp

Source: Sam Sivakumar, Intel, SPIE, Feb 2013
Litho roadmap supports cost per gate roadmap
EUV needed to enable industry target

Performance enhancement planned on the 20 nm design rule through finFET or SOI

450mm opportunity

Source: ASML
Outline

• Why EUV & 450mm

• Roadmap & scanner status
  • Roadmap
  • EUV Performance status
  • 450mm status

• Summary
Affordable shrink roadmap

- **2012**
  - Immersion
  - EUV
  - 450 mm

- **2013**
  - Immersion
  - EUV
  - 450 mm

- **2014**
  - Immersion
  - EUV
  - 450 mm

- **2015**
  - Immersion
  - EUV
  - 450 mm

- **2016**
  - Immersion
  - EUV
  - 450 mm

- **2017**
  - Immersion
  - EUV
  - 450 mm

- **2018**
  - Immersion
  - EUV
  - 450 mm

- **2019**
  - Immersion
  - EUV
  - 450 mm

- **2020**
  - Immersion
  - EUV
  - 450 mm

**EUV Immersion**
- DCO 2.5 nm $\rightarrow$ 1.0 nm
- CDU 2.0 nm $\rightarrow$ 0.6 nm
- Throughput 230 wafers per hour (wph) $\rightarrow$ >250 wph
- Resolution 27 nm $\rightarrow$ 7 nm
- EUV to immersion overlay 7.0 nm $\rightarrow$ 1.7 nm
- Throughput 69 wph $\rightarrow$ >125 wph

**QXT, QXE**
- Boost throughput measured in dies
- No cost increase per die

**Supported by a Holistic Lithography approach using computational litho, overlay and CD metrology, feedback loops.**

**Boosted throughput**
- Supported by a Holistic Lithography approach using computational litho, overlay and CD metrology, feedback loops.
NXE technology roadmap has extendibility to <7nm

<table>
<thead>
<tr>
<th>Resolution [nm]</th>
<th>32</th>
<th>27</th>
<th>22</th>
<th>16</th>
<th>13</th>
<th>10</th>
<th>7</th>
<th>&lt;7</th>
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</thead>
<tbody>
<tr>
<td>Wavelength [nm]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lens NA</td>
<td>0.25</td>
<td>0.33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Lens flare</td>
<td>8%</td>
<td>6%</td>
<td>4%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Illumination</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>coherence</td>
<td>σ=0.5</td>
<td>σ=0.8</td>
<td>σ=0.2-0.9</td>
<td>Flex-OAI</td>
<td>Extended Flex-OAI</td>
<td>reduced pupil fill ratio</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overlay DCO [nm]</td>
<td>7</td>
<td>4.0</td>
<td>3.0</td>
<td>1.5</td>
<td>1.2</td>
<td>1.0</td>
<td></td>
<td></td>
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<tr>
<td>MMO [nm]</td>
<td>7.0</td>
<td>5.0</td>
<td>2.5</td>
<td>2.0</td>
<td>1.7</td>
<td></td>
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<tr>
<td>TPT Dose [mJ/cm²]</td>
<td>5</td>
<td>10</td>
<td>15</td>
<td>15</td>
<td>20</td>
<td>20</td>
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<tr>
<td>Power [W]</td>
<td>3</td>
<td>10 - 105</td>
<td>80 - 250</td>
<td>250</td>
<td>250</td>
<td>500</td>
<td></td>
<td></td>
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<tr>
<td>Throughput [w/hr]</td>
<td>-</td>
<td>6 - 60</td>
<td>50 - 125</td>
<td>125</td>
<td>125</td>
<td>165</td>
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</table>
# ASML’s NXE:3100 and NXE:3300B

<table>
<thead>
<tr>
<th>Feature</th>
<th>NXE:3100</th>
<th>NXE:3300B</th>
</tr>
</thead>
<tbody>
<tr>
<td>NA</td>
<td>0.25</td>
<td>0.33</td>
</tr>
<tr>
<td>Illumination</td>
<td>Conventional 0.8 σ</td>
<td>Conventional 0.9 σ Off-axis illumination</td>
</tr>
<tr>
<td>Resolution</td>
<td>27 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>Dedicated Chuck Overlay / Matched Maching Overlay</td>
<td>4.0 nm / 7.0 nm</td>
<td>3.0 nm / 5.0 nm</td>
</tr>
<tr>
<td>Productivity</td>
<td>6 - 60 Wafers / hour</td>
<td>50 - 125 Wafers / hour</td>
</tr>
<tr>
<td>Resist Dose</td>
<td>10 mJ / cm²</td>
<td>15 mJ / cm²</td>
</tr>
</tbody>
</table>
Eleven NXE:3300B systems in various states of integration
new clean room completed in July ‘12
NXE:3300B imaging and overlay beyond expectations
Matched overlay to immersion ~3.5 nm

Scanner qualification

22nm HP
BE = 15.9 mJ/cm²
EL = 13%
DoF = 160 nm
Full wafer CDU = 1.5nm

Scanner capability

13 nm HP
18 nm HP
9 nm HP

Single exposure
EUV Spacer

Matched Machine Overlay

Lot (1.3,1.3)

Lot (3.4,3.0)

Matched Chuck

Day

Lot

1
2
3

1.3
1.0
1.2
1.4
1.4
1.3

1.3
1.0
1.2
1.4
1.4
1.3

XT:1950i reference wafers
EEXY sub-recipes
16par (avg. field) +
CPE (6 par per field)

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Matched Chuck

Day

Lot

1
2
3

1.3
1.0
1.2
1.4
1.4
1.3

1.3
1.0
1.2
1.4
1.4
1.3

XT:1950i reference wafers
EEXY sub-recipes
16par (avg. field) +
CPE (6 par per field)
EUV source: repeatable stable performance, dose in spec
250 W target to be reached in 2015

80W enabled by 3300 drive laser
250W enabled by high-power drive & seed laser, 1µm separate pre-pulse, 80kHz droplet generator

Total 20 hours 40W & 50W runs with good dose reproducibility:
99.7% of the dies < 0.5% dose

20 hour runs total representing
~ 830 exposed wafers @ 15 mJ/cm²

55W run (97.5% of dies in spec) to test peak performance
NXE:3300B systems have started shipping
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Summary

• Cost effective scaling in lithography enabled by:
  • Immersion performance improvement in imaging, overlay & productivity
  • EUV at 0.33NA for ultimate shrink capability & potential device performance, starting with device production in 2014
  • 450mm for further cost reduction opportunity, targeted to start device production in 2018

• EUV roadmap & scanner status
  • NXE:3100 in use for process/device development at customers with positive results
  • NXE:3300B has started shipping and meets imaging and overlay targets
  • Industrialization progress demonstrated towards 70 WPH in 2014
  • Roadmap to <7nm with 0.33NA + extensions & double patterning &/or higher NA

• 450mm roadmap & scanner status
  • 450 mm looks like a doable cost reduction scenario, but the litho-specific cost reduction will be limited, considering that productivity scales fundamentally negatively with the wafer surface
  • ASML has initiated 450 mm program, early version systems from 2015 using EUV systems and 2016 for immersion systems, significant enhancements required.
  • Concerns remain regarding limited overall industry 450 mm implementation plans
Thank you!