ASML

Cost effective scaling: next-generation lithography progress and prospects

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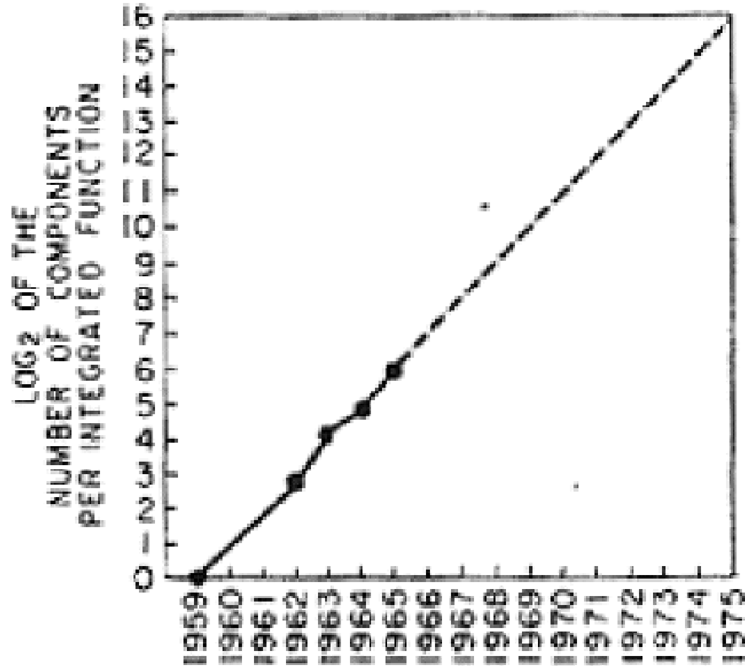
Sokudo Breakfast Forum
Semicon West

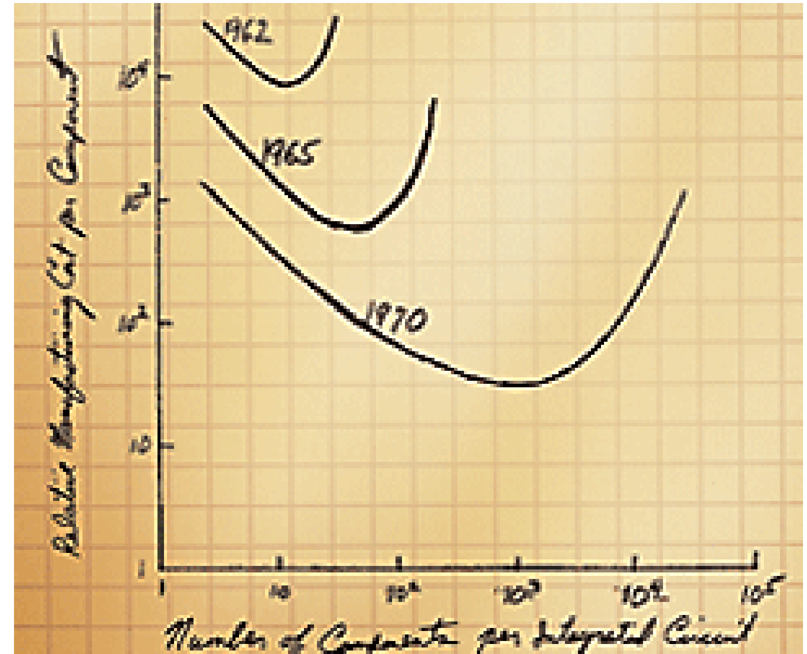
July 10th, 2013

Outline

- Why EUV & 450mm
- Roadmap & scanner status
  - Roadmap
  - EUV performance status
  - 450mm status
- Summary

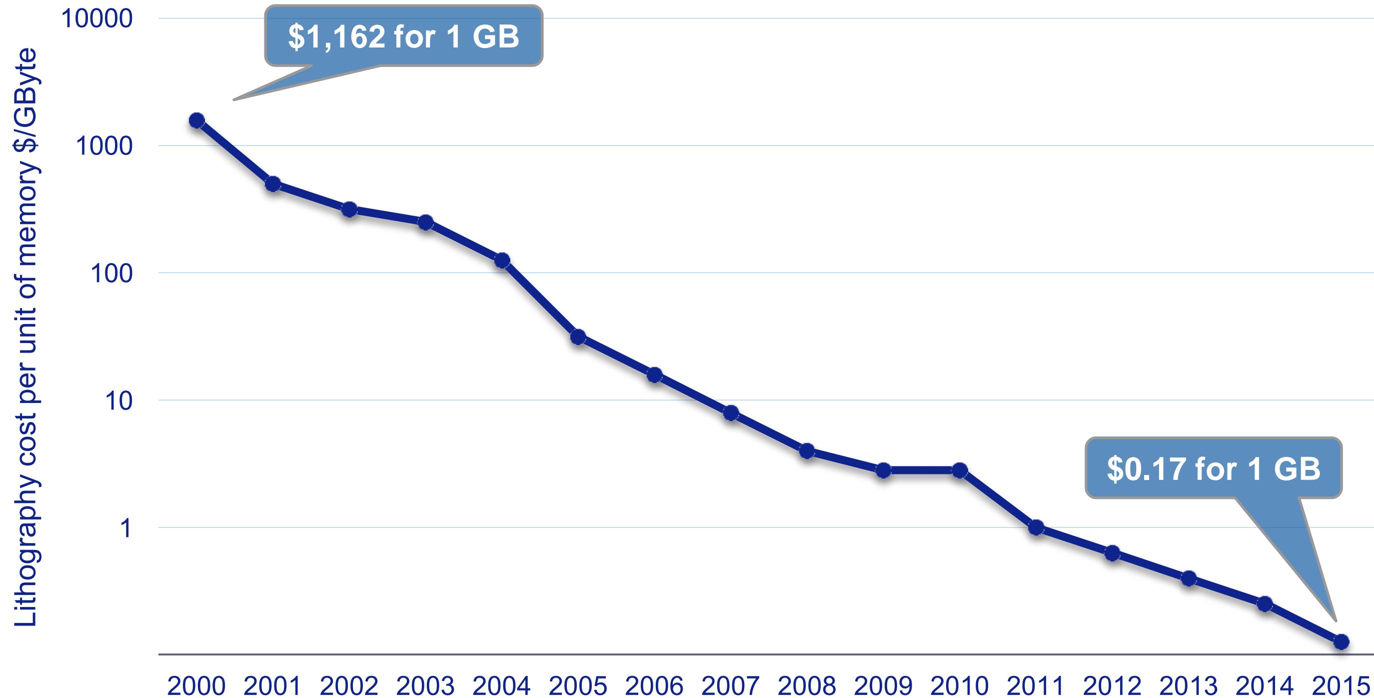
Moore’s law : *Doubling of components per chip every 12 months resulting in a lower cost per component*





"Cramming more components onto integrated circuits“, *Electronics Magazine April 19, 1965*

Moore's Law: what it means for consumers



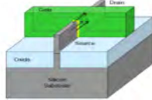
Source: Gartner. High quality Flash

IC manufacturers' roadmaps supports further device scaling

Logic

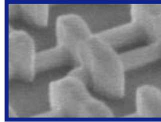
2012 - 2013: 22 - 20nm node

Memory: 0.09um2, SRAM
Device: planar or FinFET (Intel)
Gate: RMG-HKMG
Channel: Si
Vdd: 0.8V



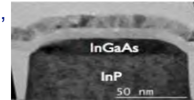
2014 - 2015: 16 - 14nm node

Memory: 0.08um2 SRAM
Device: FinFET, FDSOI
Gate: RMG-HKMG
Channel: Si; (Si)Ge
Vdd: 0.6V



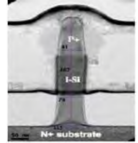
2016 - 2017: 11 - 10nm node

Memory: 0.06um2 SRAM
Device: FinFET
Gate: HKMG
Channel: Si, Ge, IIIVr
Vdd: 0.5V



2018 - 2019: 8 - 7nm node

Memory: FBRAM, STT-RAM, >8TSRAM
Device: FinFET, Nanowire, TFET
Gate: HKMG
Channel: IIIV-Graphene



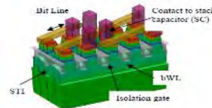
DRAM

2012 - 2013: 38 - 32nm node

Memory: stacked MIM
Peri: planar
Array: 6F2, bWL
Gate: poly/SiO2
Channel: Si
Vdd=1.35V

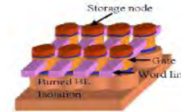
2014 - 2015: 29 - 22nm node

Memory: stacked MIM
Peri: planar HKMG
Array: 6F2, bWL
Gate: HKMG
Channel: Si
Vdd=1.2V



2016 - 2017: 22 - 16nm node

Memory: stacked MIM
Peri: planar
Array: 6F2, 4F2, bBL, LBL, 1T1C(VFET)
Gate: HKMG
Channel: Si
Vdd=1.1V



2018 - 2019: 16 - 14nm node

Memory: FBRAM, STT-MRAM, RRAM, PcRAM
Peri: planar
Array: 4F2, 1T, 1T1R, 1T1MTJ(VFET)
Gate: HKMG
Channel: Si
Vdd~1V

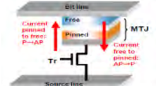
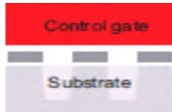


Fig. 1 Writing operation of 1T/1M STT-MRAM cell.

Flash

2012 - 2013: 19 - 16nm hp

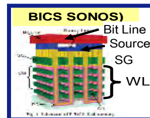
4.5F - 6F2 asymm. cell
Density: 128G
Device: FG



2014 - 2015: 16 - 13nm hp

3D NAND intro at 5x → 4xnm

6F2 asymmetric cell
4F2 symmetric cell
Density: 256-512G
Device: dual-FG



2016 - 2017: ~ 11nm hp (planar)

3D NAND at 3x → 2xnm X-pt intro at 2xnm

7F2 asymmetric cell
4F2 symmetric cell
Density: 512-1024G
Device:: dual-FG, BiCS in HVM(@4xnm)

2018 - 2019: < 10nm hp (planar)

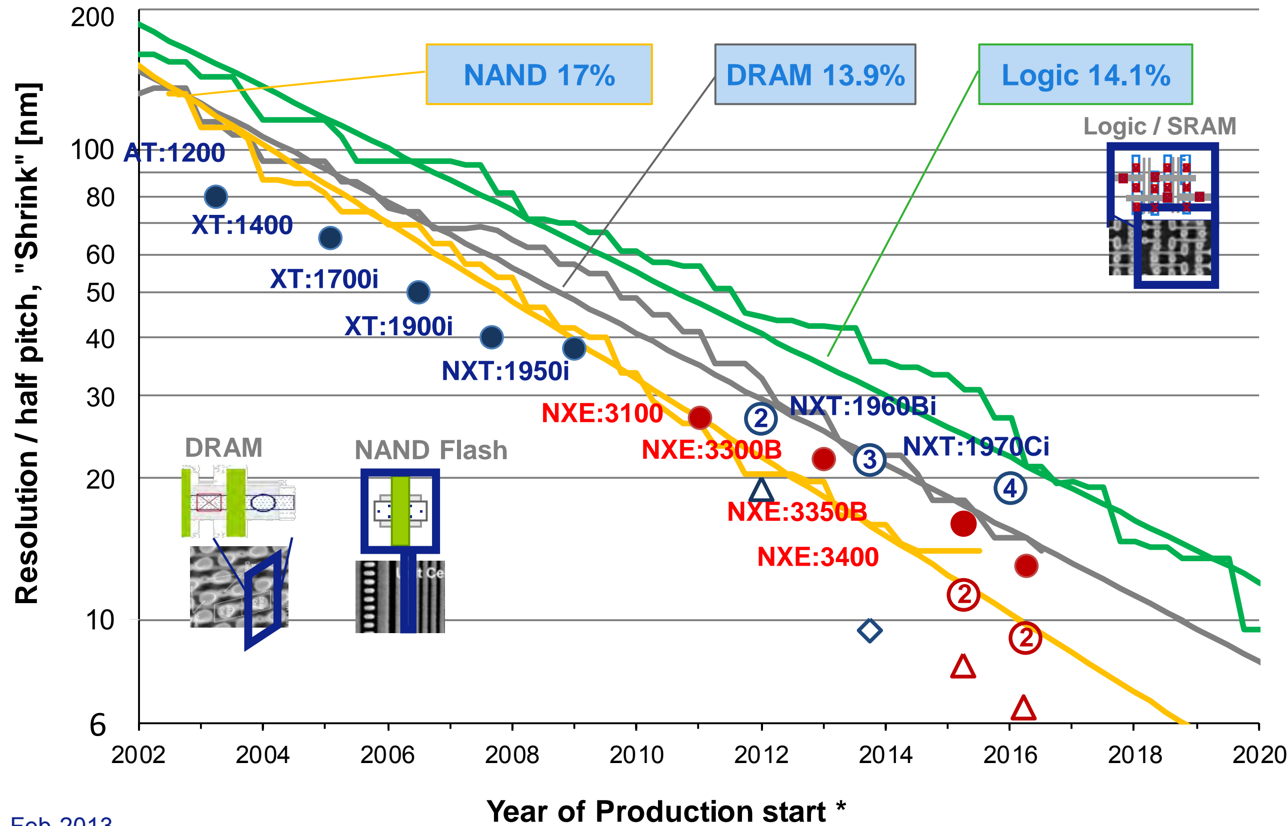
X-pt intro at 2xnm

Density: > 1T with 3D chip stacking
Device: 3D BiCS, XPoint-RRAM
Selector: diode

Source: IMEC, ASML TDC, Jan 2013

Industry roadmap towards <10 nm resolution

Lithography roadmap supports continued shrink



- Single Exposure
- ⓝ 2D LE^n Patterning
- △ 1D SADP
- ◇ 1D SAQP
- DUV
- EUV

LE = Litho-Etch, n = number of iterations

SADP = Self Aligned Double Patterning

SAQP = Self Aligned Quadruple Patterning

* Note: Process development 1.5 ~ 2 years in advance

Cost becomes a concern post 28 nm

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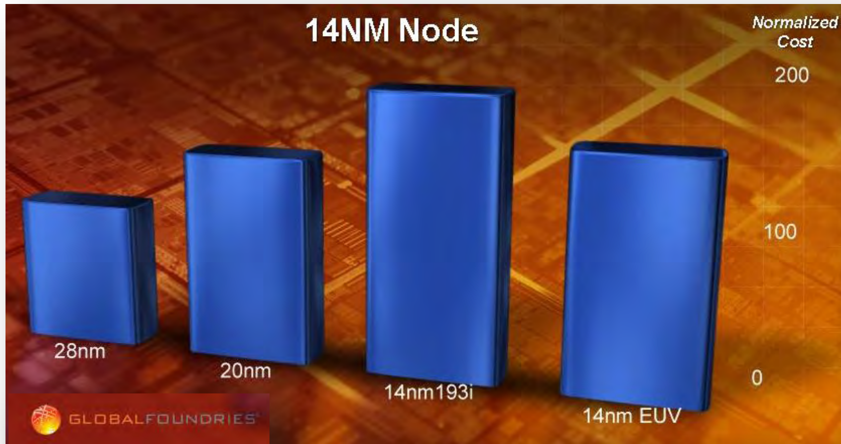
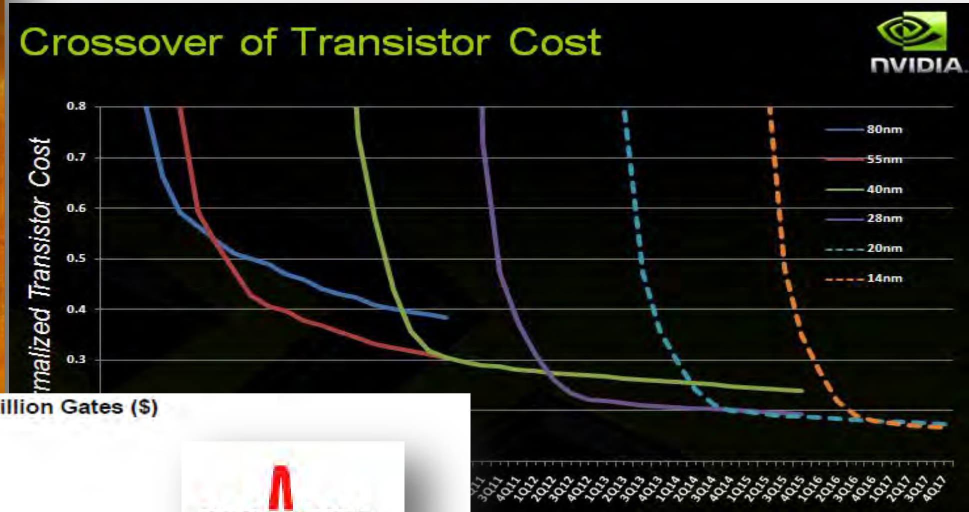
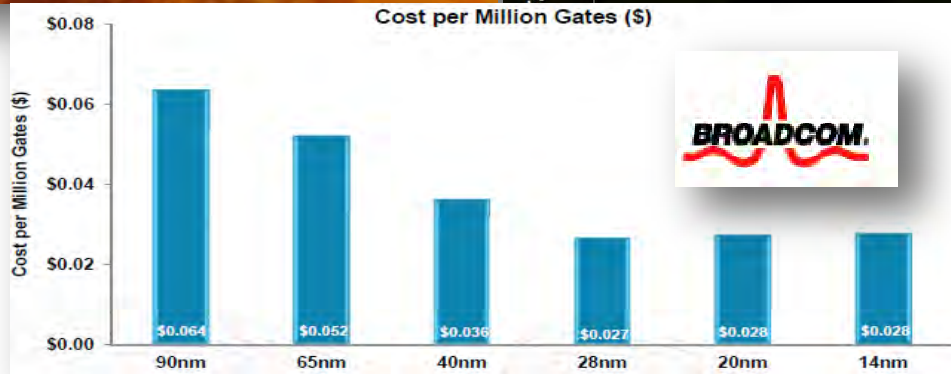
Public



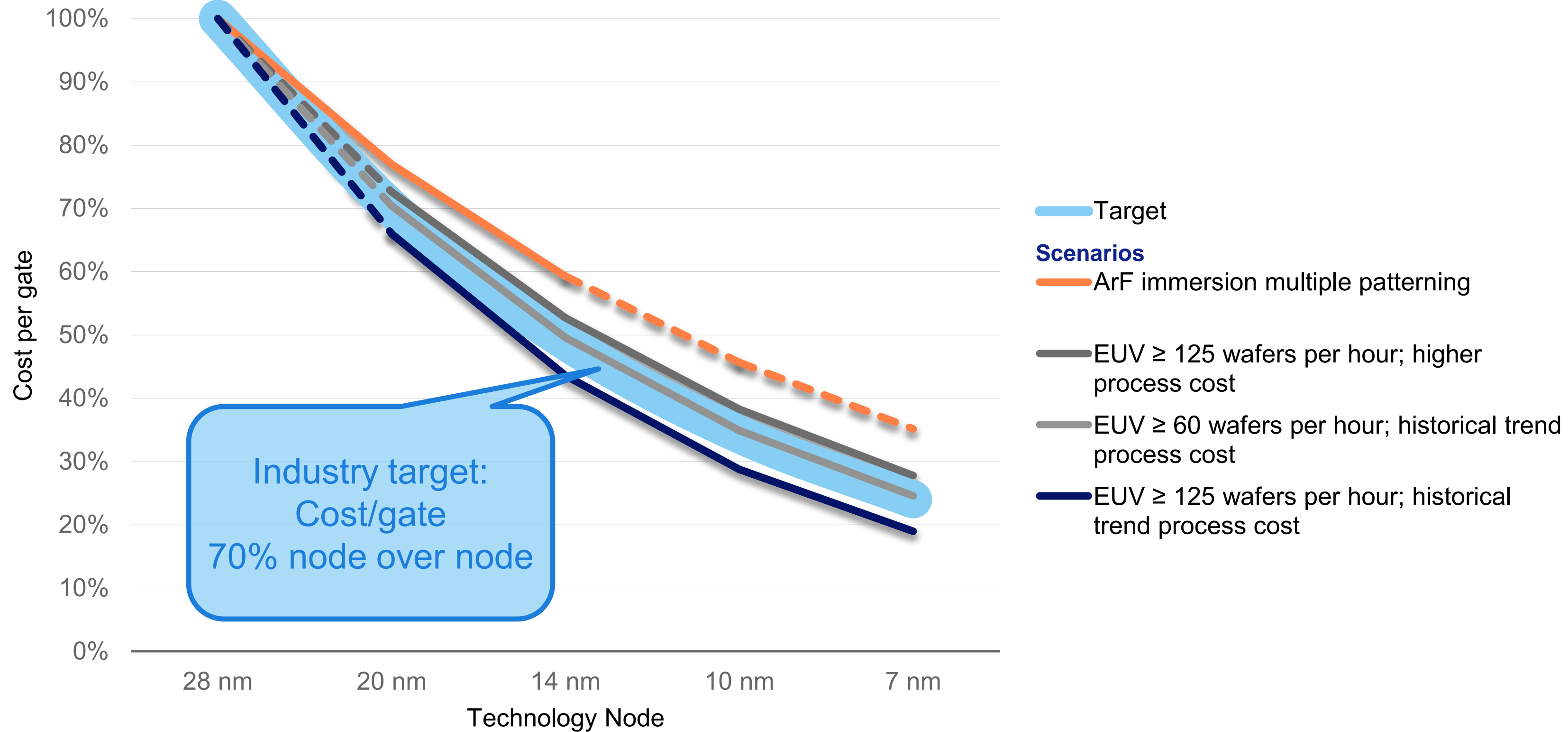




Sources: nVidea, ITPC, nov, 2011
Broadcom, IMEC, may 2012
GF, ISS, jan 2013

Litho roadmap supports cost per gate roadmap

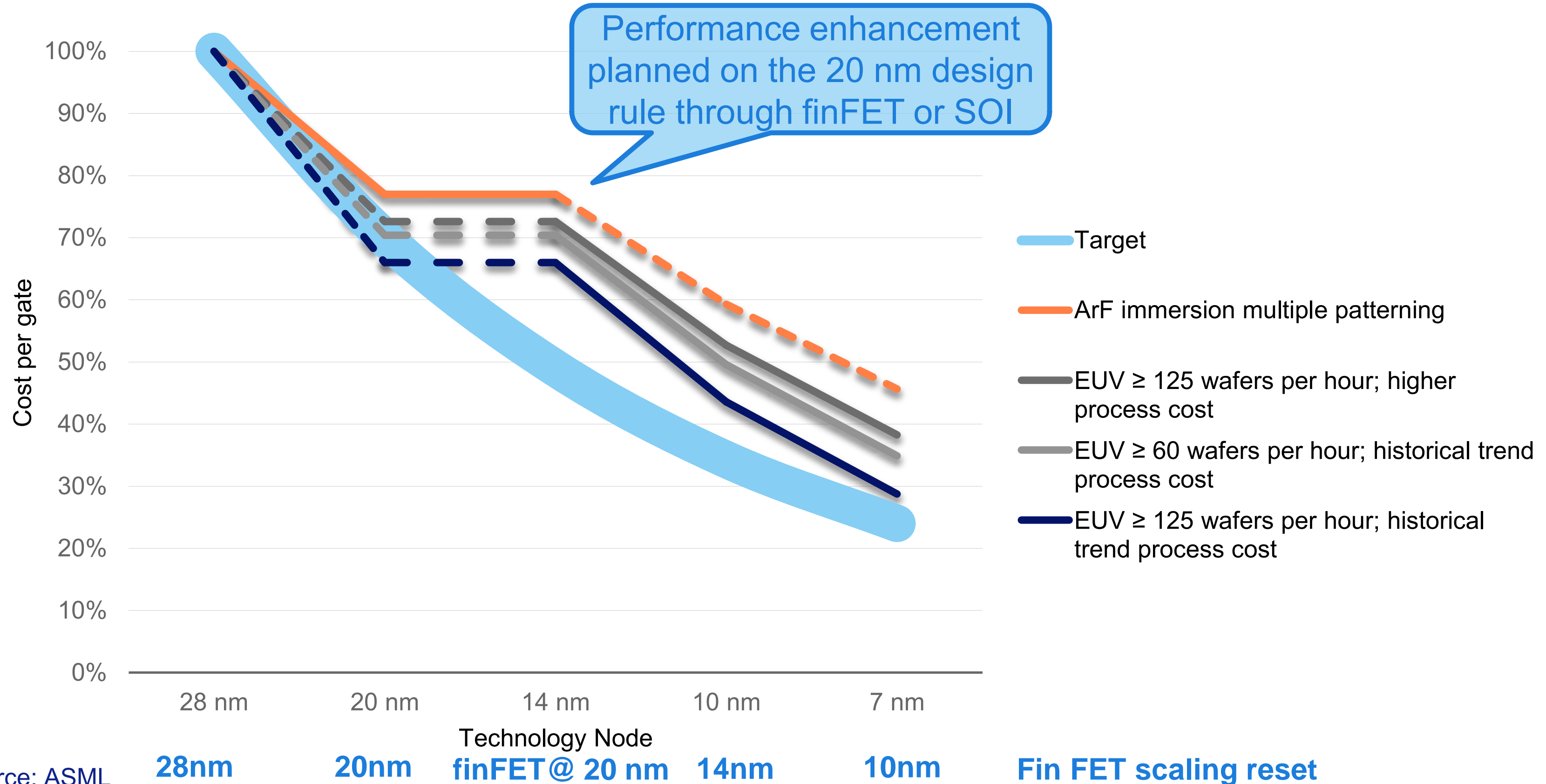
EUV needed to enable industry target



Source: ASML

Litho roadmap supports cost per gate roadmap

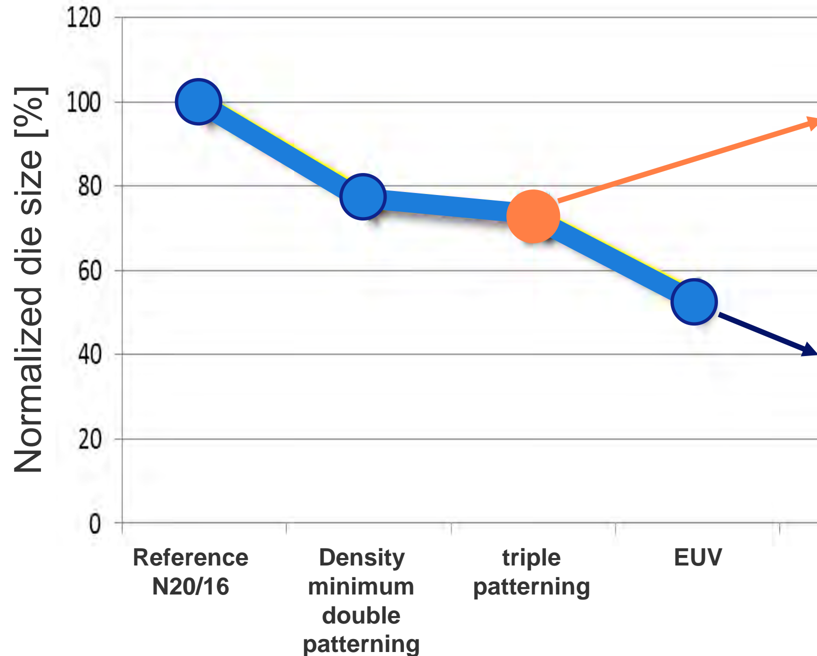
EUV needed to enable industry target

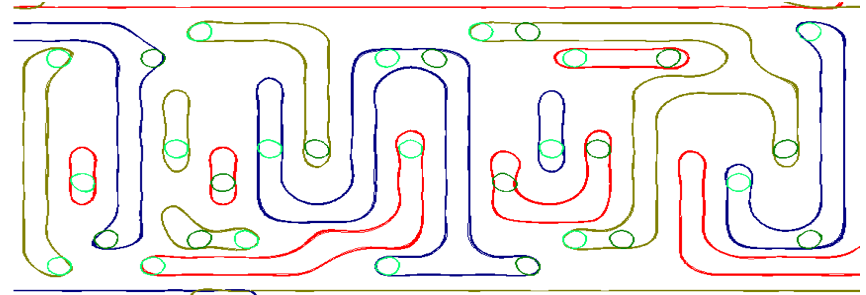


Source: ASML

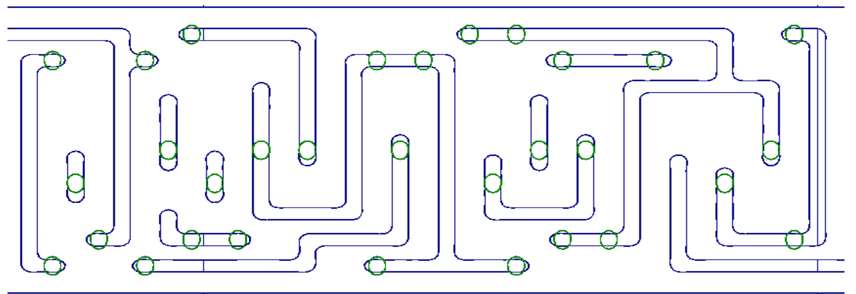
Only EUV can enable 50% scaling for the 10 nm node

Layout restrictions and litho performance limit shrink to ~25% using immersion





Triple patterning does not show an process window

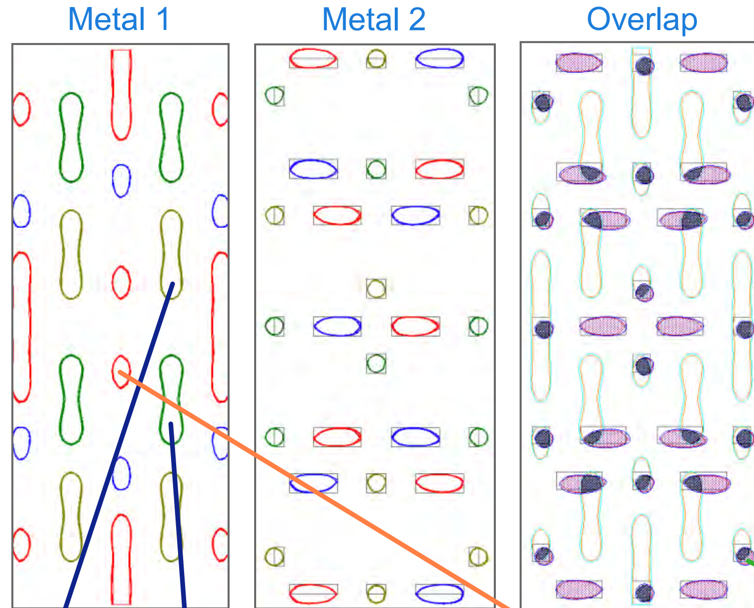


EUV meets all litho requirements

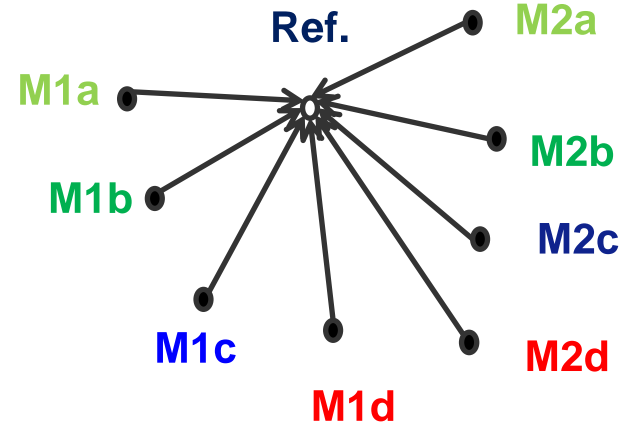
Source: ARM, Scaled N20 nm flip-flop design

Even gridded SRAM designs prefer EUV at 10 nm

Limited overlay between local interconnect layers makes multiple patterning very difficult



All exposures have to match to each other to enable sufficient Metal 1 to 2 overlap, leading to tight overlay requirements



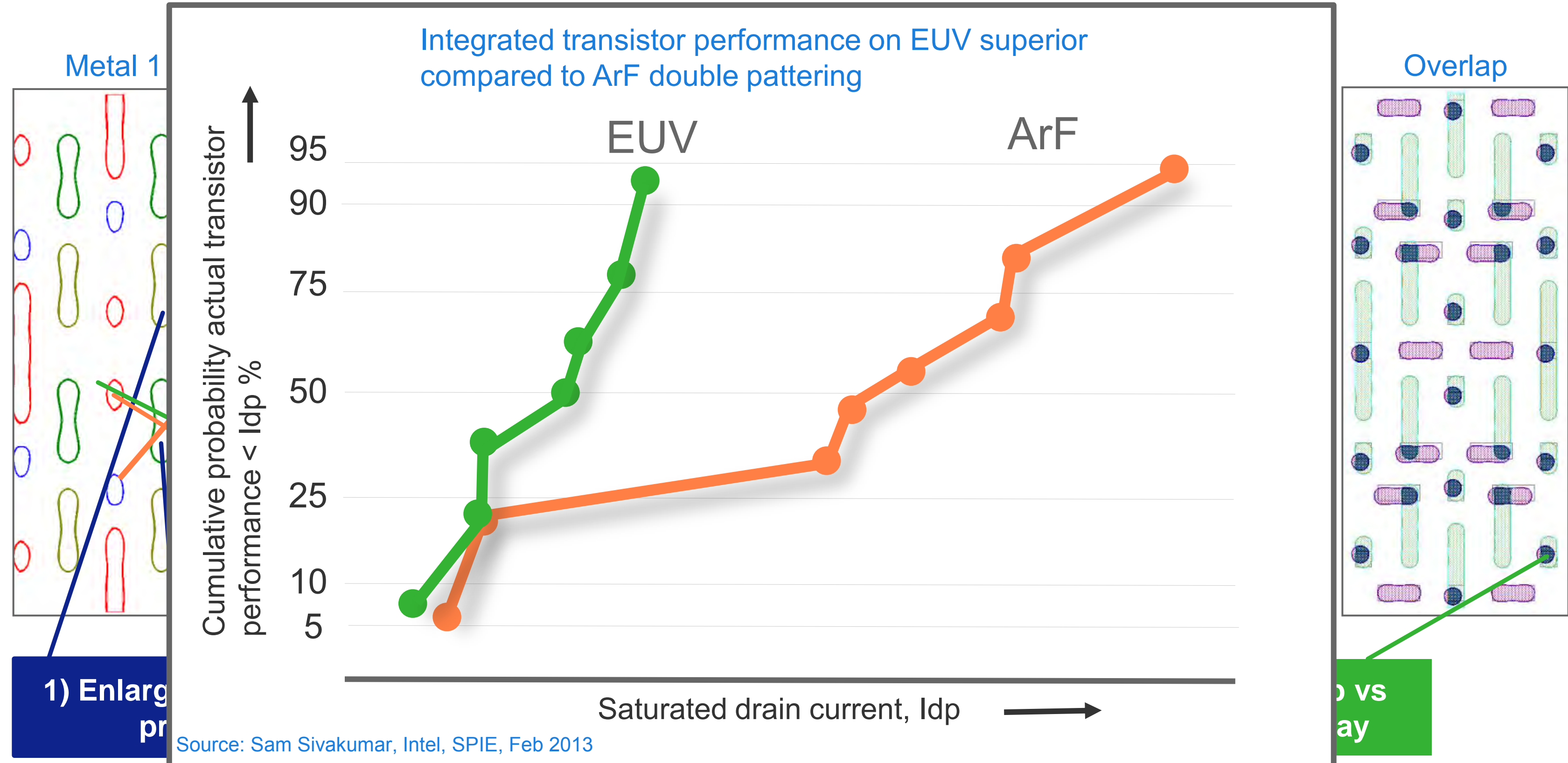
1) Small overlapping process window

2) Marginal CD control

3) Failing overlap at 3 nm overlap

Even gridded SRAM designs prefer EUV at 10 nm

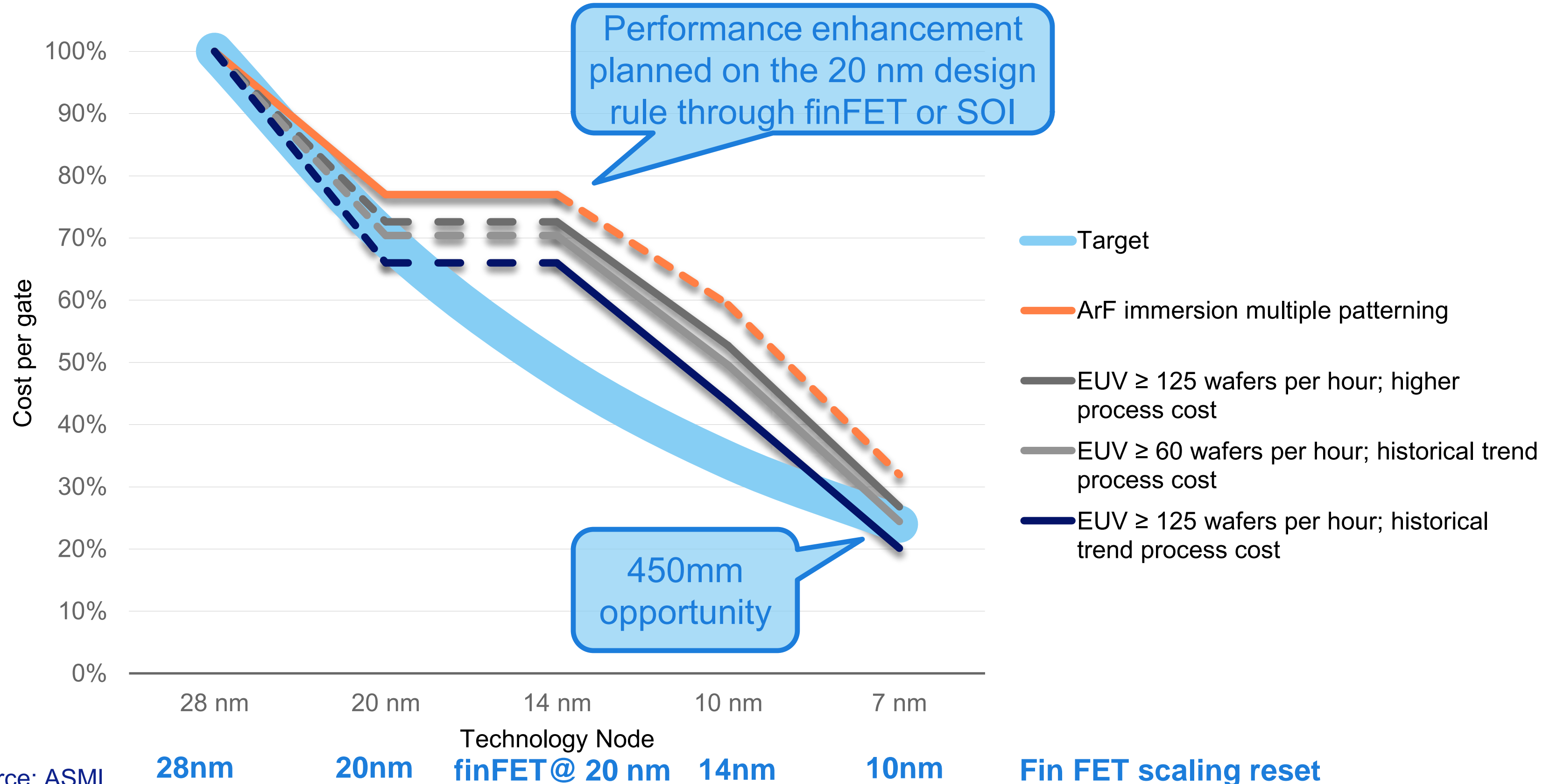
Limited overlay between local interconnect layers makes multiple patterning very difficult



Source: Sam Sivakumar, Intel, SPIE, Feb 2013

Litho roadmap supports cost per gate roadmap

EUV needed to enable industry target



Source: ASML

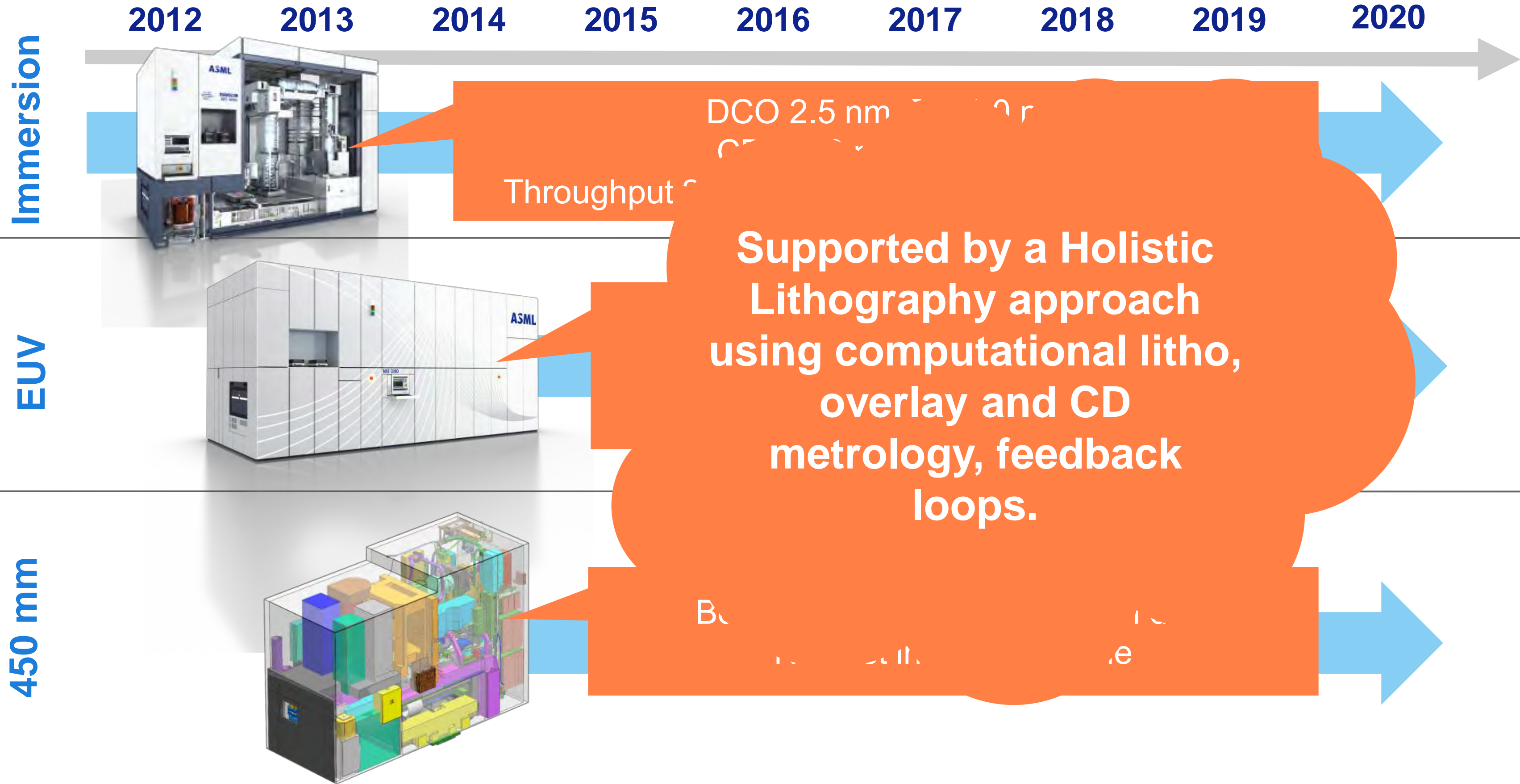
Outline

- Why EUV & 450mm
- **Roadmap & scanner status**
  - **Roadmap**
  - **EUV Performance status**
  - **450mm status**
- Summary

Affordable shrink roadmap

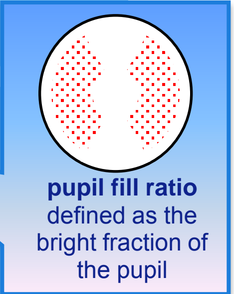
Public

Slide 15



NXE technology roadmap has extendibility to <7nm

						Under study			
Resolution [nm]		**32**	**27**	**22**	**16**	**13**	**10**	**7**	**<7**
Wavelength [nm]		13.5							
Lens	NA	0.25		0.33			0.33NA DPT		0.45-0.60 DPT
							0.45	0.60	
	flare	8%		6%	4%				
Illumination	coherence	σ=0.5	σ=0.8	σ=0.2-0.9	Flex-OAI	Extended Flex-OAI			
						reduced pupil fill ratio			
Overlay	DCO [nm]	7	4.0	3.0	1.5	1.2	1.0		
	MMO [nm]	-	7.0	5.0	2.5	2.0	1.7		
TPT (300mm)	Dose [mJ/cm^2]	5	10	15	15	20	20		
	Power [W]	3	10 - 105	80 - 250	250	250	500		
	Throughput [w/hr]	-	6 - 60	50 - 125	125	125	165		



ASML's NXE:3100 and NXE:3300B

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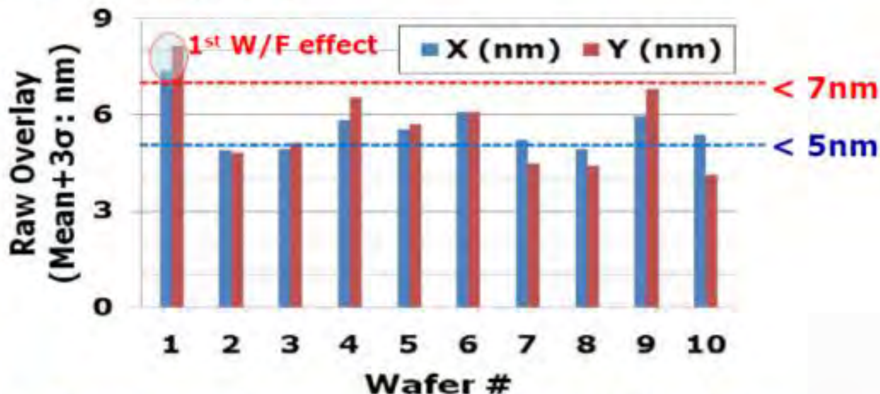
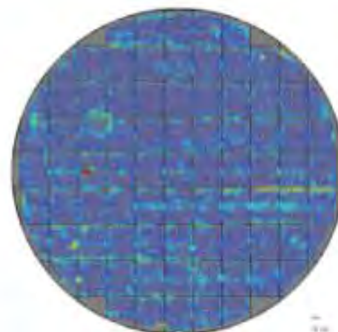
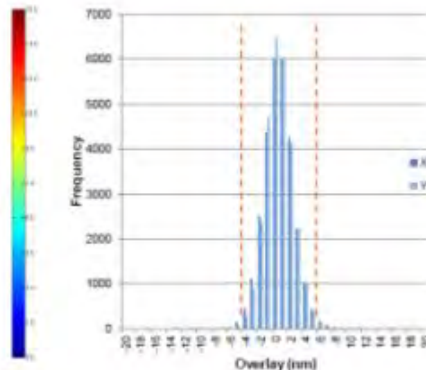
	NXE:3100	NXE:3300B
NA	0.25	0.33
Illumination	Conventional 0.8 σ	Conventional 0.9 σ Off-axis illumination
Resolution	27 nm	22 nm
Dedicated Chuck Overlay / Matched Maching Overlay	4.0 nm / 7.0 nm	3.0 nm / 5.0 nm
Productivity	6 - 60 Wafers / hour	50 - 125 Wafers / hour
Resist Dose	10 mJ / cm2	15 mJ / cm2

NXE:3100 imaging & overlay performance at customers



Eleven NXE:3300B systems in various states of integration new clean room completed in July ‘12

System 1

Development tool

System 9

System 2

System 6

System 3

New cleanroom

System 7

System 4

System 5

System 8

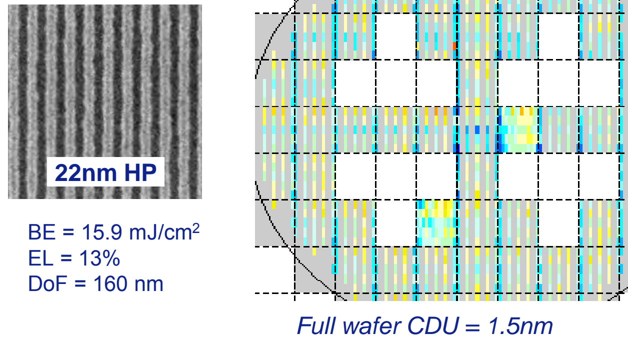
System 10
Training

System 11

NXE:3300B imaging and overlay beyond expectations

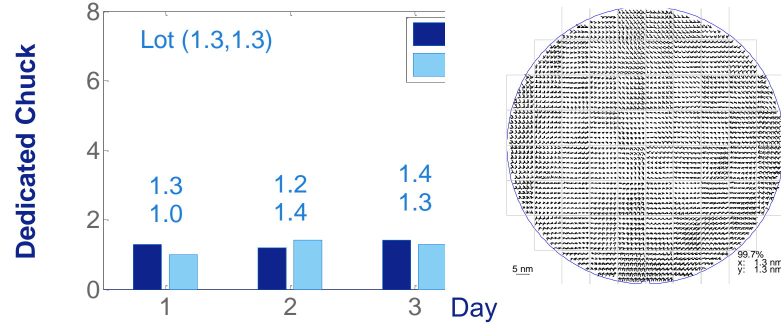
Matched overlay to immersion ~3.5 nm

Scanner qualification

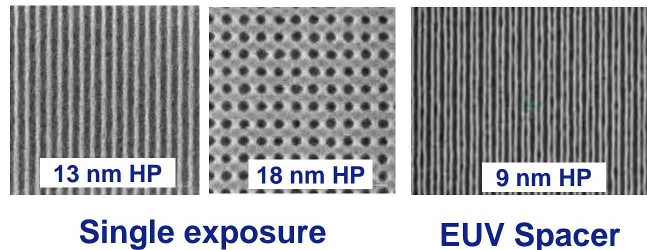


BE = 15.9 mJ/cm²
EL = 13%
DoF = 160 nm

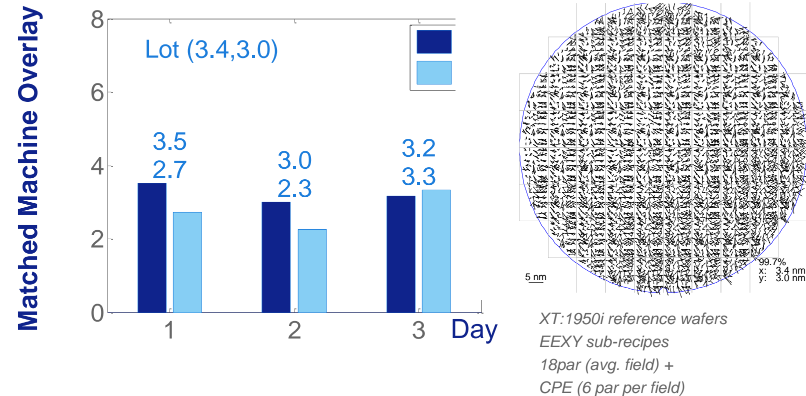
Full wafer CDU = 1.5nm



Scanner capability



Single exposure **EUV Spacer**



XT:1950i reference wafers
EEXY sub-recipes
18par (avg. field) +
CPE (6 par per field)

EUV source: repeatable stable performance, dose in spec

250 W target to be reached in 2015

1000
100
10
1

Power [W]
Productivity [Wafers/hr]

2008 2009 2010 2011 2012 2013 2014 2015 2016

2 5 10 30 40 55 80 125 250
43 58 81 126

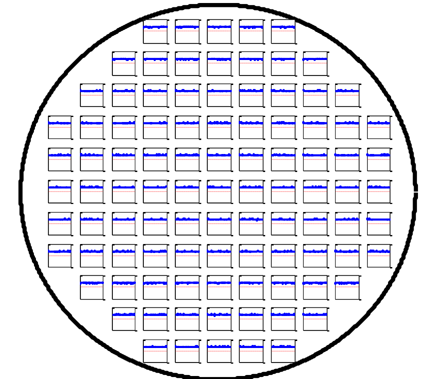
250W enabled by high-power drive & seed laser, 1µm separate pre-pulse, 80kHz droplet generator

80W enabled by 3300 drive laser

Total 20 hours 40W & 50W runs with good dose reproducibility: 99.7% of the dies < 0.5% dose

20 hour runs total representing ~ 830 exposed wafers @ 15 mJ/cm²

55W run (97.5% of dies in spec) to test peak performance



NXE:3300B systems have started shipping

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Summary

- **Cost effective scaling in lithography enabled by:**
  - Immersion performance improvement in imaging, overlay & productivity
  - EUV at 0.33NA for ultimate shrink capability & potential device performance, starting with device production in 2014
  - 450mm for further cost reduction opportunity, targeted to start device production in 2018

- **EUV roadmap & scanner status**
  - NXE:3100 in use for process/device development at customers with positive results
  - NXE:3300B has started shipping and meets imaging and overlay targets
  - Industrialization progress demonstrated towards 70 WPH in 2014
  - Roadmap to <7nm with 0.33NA + extensions & double patterning &/or higher NA

- **450mm roadmap & scanner status**
  - 450 mm looks like a doable cost reduction scenario, but the litho-specific cost reduction will be limited, considering that productivity scales fundamentally negatively with the wafer surface
  - ASML has initiated 450 mm program, early version systems from 2015 using EUV systems and 2016 for immersion systems, significant enhancements required.
  - Concerns remain regarding limited overall industry 450 mm implementation plans

ASML

Thank you!