



“Shooting for the 22nm Lithography Goal” with the

SOKUDO DUO
Coat/Develop Track

Three (3) different exposure options for 22nm:

- **MAPPER Lithography on E-Beam Maskless (ML2)**
- **ASML on EUV Lithography & M.P. Immersion ArF**
- **NIKON on Multiple Patterning Immersion ArF & EUVL**

One (1) in-line coat/develop track fits all scenarios:



However, coat/develop track configuration varies significantly by photolithography technology ...

Throughput (wph) Projections

wph = wafers per hour

* Assumes E-Beam (ML2) Cluster Tool such as MAPPER Litho.

	2011	2012	2013	2014	2015
E-Beam	1 – 5	5 – 10	60 – 100*	100+*	120+*
EUV	30 – 60	60 – 100	80 – 125	125+	150+
Immersion	180 – 230	200 – 240	220 – 260	260+	280+

22NM
VOLUME
RAMP

NECESSARY FOR IMMERSION
DOUBLE / MULTI-PATTERNING
TO BE COST-EFFECTIVE

Resist Process Steps on Track

	UL / Barc Coat	Resist Coat	Top Coat	Backside Clean	Bevel Clean	Post E. Rinse	Deve-lope
E-Beam	■	■	-	■	-	-	■
EUV	■	■	-	■	-	-	■
Immersion	■	■	▲	▲	■	■	■

SOKUDO Coat/Develop Track 22nm Process Development

imec Double Patterning LPLE

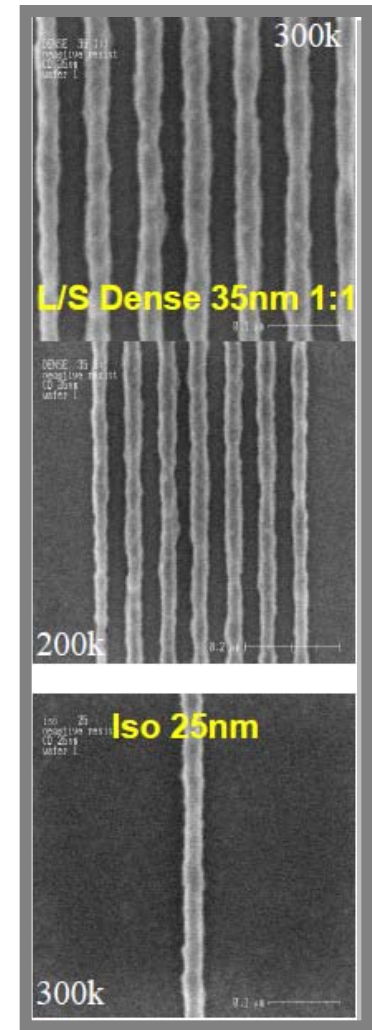
➤ Materials & Process Benchmarking 32nm → 26nm

Selete EUV Lithography Resist Qual.

➤ New resist process evaluations @ SELETE

cea leti E-Beam DW Qualification

➤ MAPPER Lithography E-Beam Process R&D



SOKUDO RF3 track process
E-Beam litho. exposures on
Vistec SB3054DW at LETI

SOKUDO DUO

imec Immersion Lithography with SOKUDO

- ◆ Immersion Resist Process Defectivity: Microbridging & Resist Filtration
- ◆ CoO Study for Double Patterning Lithography
- ◆ **CDU optimization for immersion lithography & Double Patterning:**
 - JSR's litho-freeze-litho process (freeze coat, thermal freeze)
 - TOK's posi-posi process "Freeze-Free"

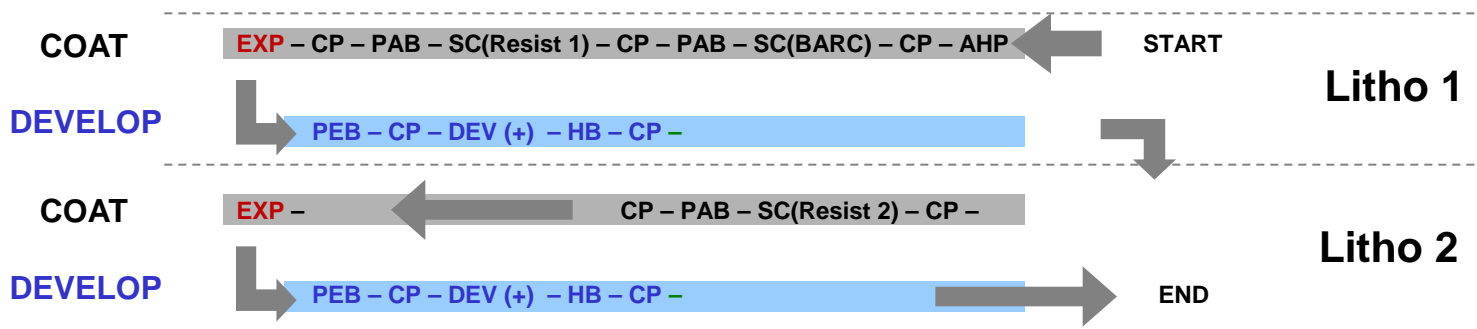


ASML XT:1900Gi + SOKUDO RF3S

“Photo” Double Patterning Resist Process on Track

	Freeze Coat chemical b/w 1 st & 2 nd Resist	Self-Freeze by 2 nd Resist Coat & Bake	Thermal freeze bake
JSR	☺	--	☺
TOK	--	☺	--
Dow Elec. Mtrl.	○		○
Shin-Etsu	--		○
Sumitomo	--		○

TOK Freeze-Free or
JSR Thermal Freeze





JSR Freeze Coat & Thermal Freeze Comparison

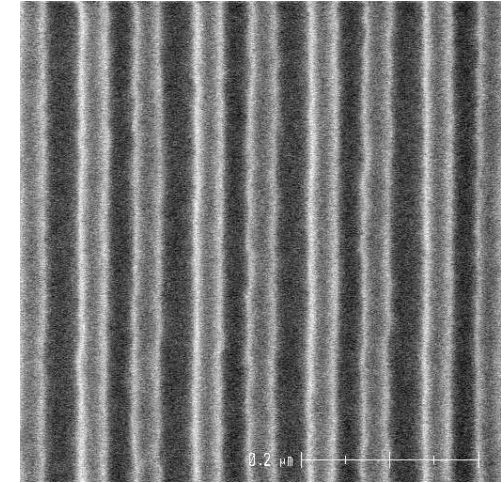
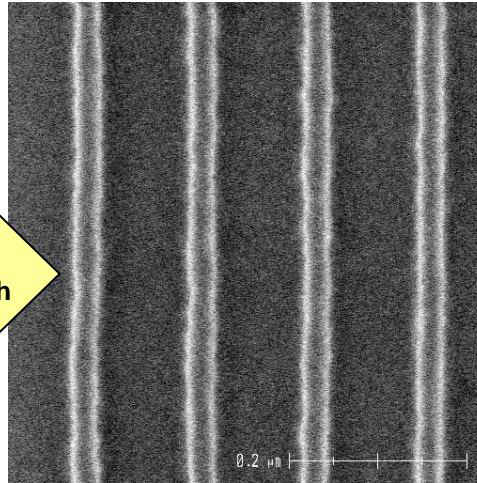
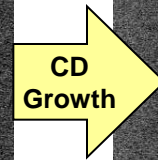
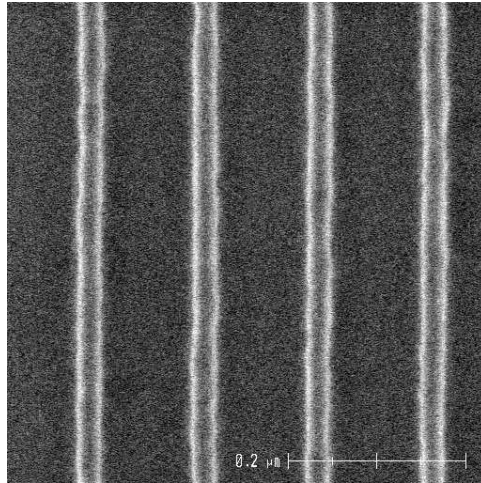
32nm Feature Target CD-SEM Images

Litho 1 @ L1

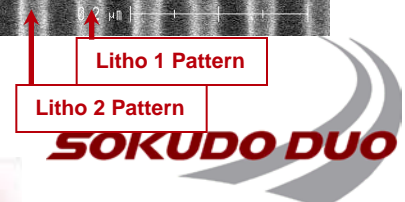
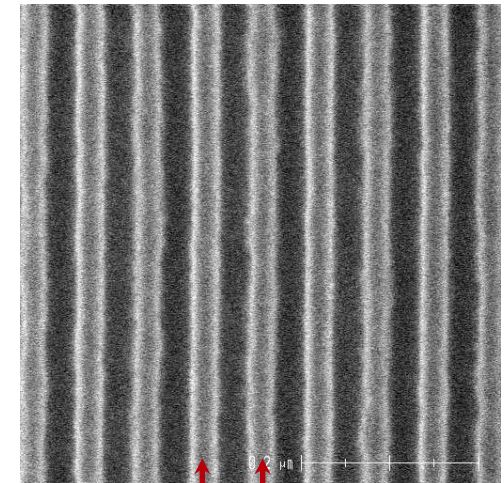
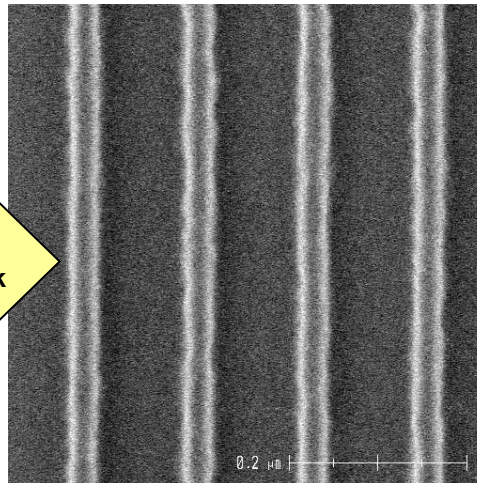
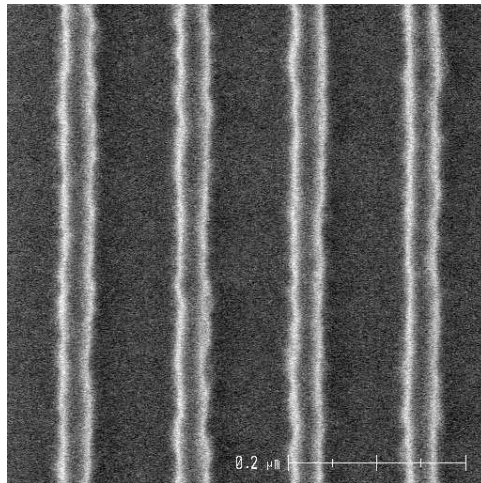
Litho 1 @ L2

Combined L1:L2 Pattern

Freeze Coat



Thermal Freeze

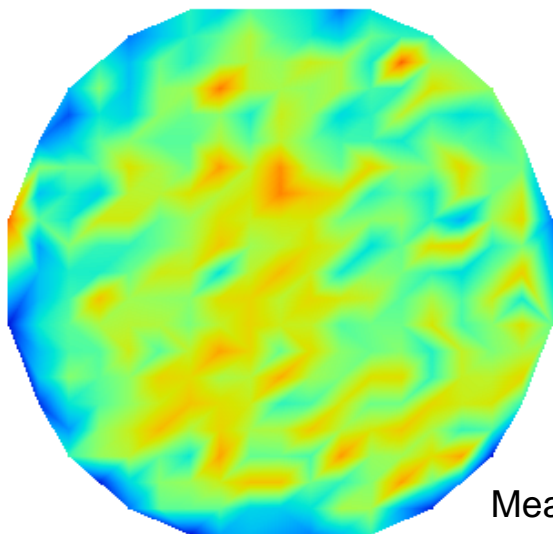


JSR Thermal-Freeze 26nm L/S Target CDU

SPIE 7639-81 Simplified "Litho-Cluster-Only" solution for double patterning ; JSR, ASML, SOKUDO

The CD uniformity data with the thermal freeze process comparable to traditional litho-etch-litho-etch and spacer double patterning CDU.

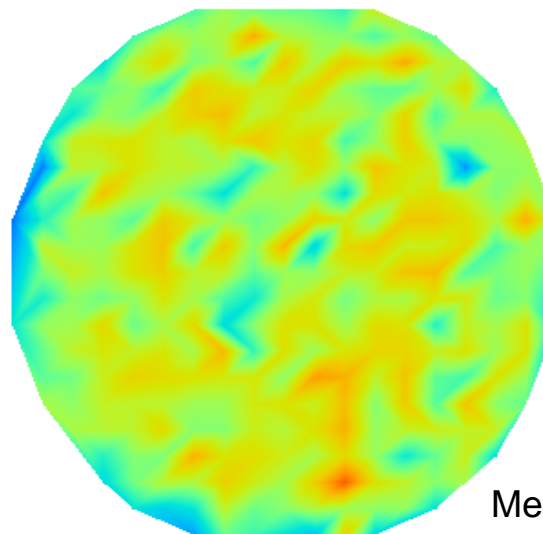
Layer 1



Mean : 27.00nm
CDU 3 σ : 1.85nm



Layer 2



Mean : 26.75nm
CDU 3 σ : 1.35nm



Substrate:ARC@29-SR (105nm)

Layer 1 : Non-TC thermal freeze resist (FT=60nm,130C/125C, SCA/RCA/ACA=90° /76° /94°)

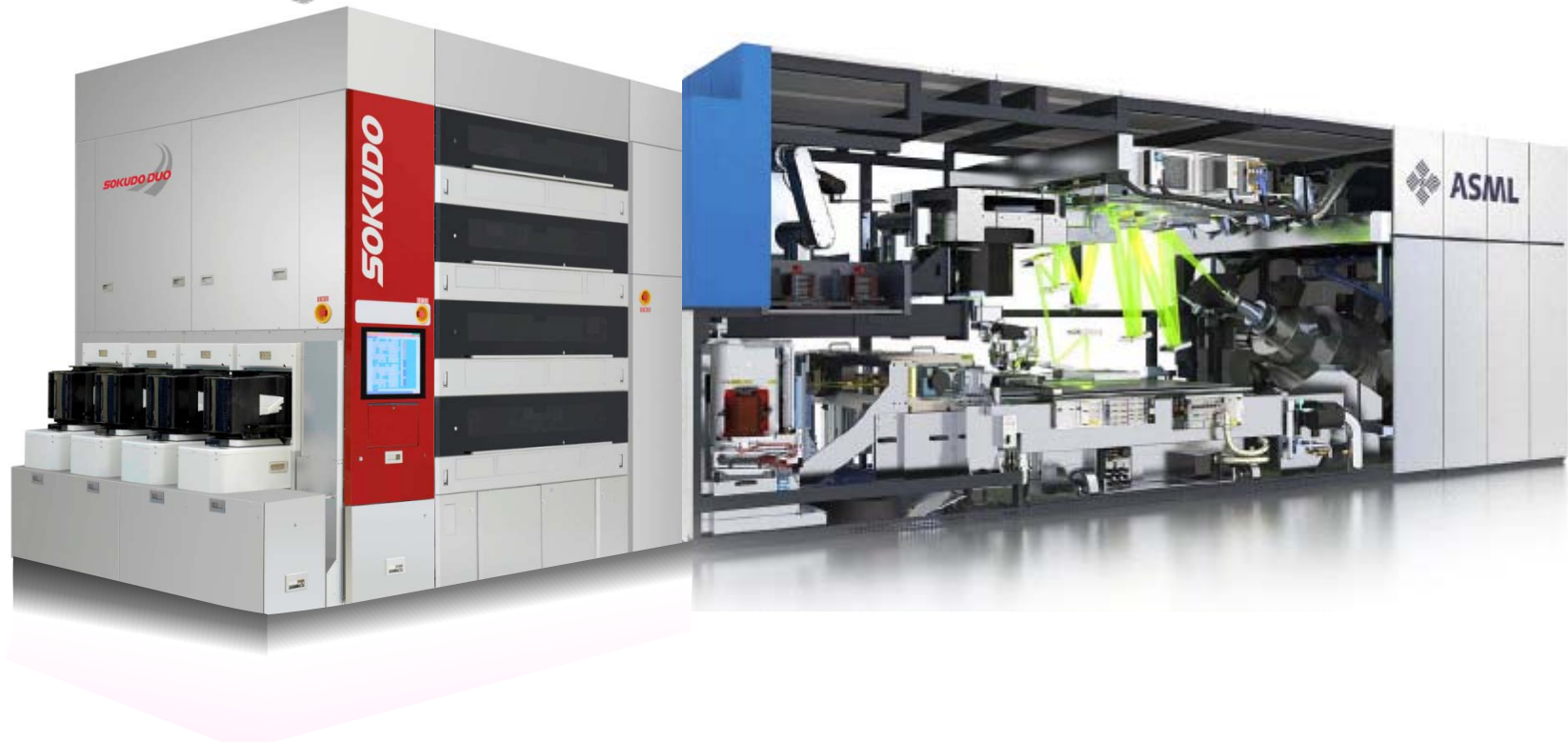
Layer 2 : Non-TC normal resist (FT=50nm,100C/95C, SCA/RCA/ACA=92° /80° /95°),

Exposure : 39nmL96nP with att-PSM, NA=1.35, Dipole40X, 0.747/0.626, Y-Polarization

Development : ECO Nozzle(OPD262/DIW)

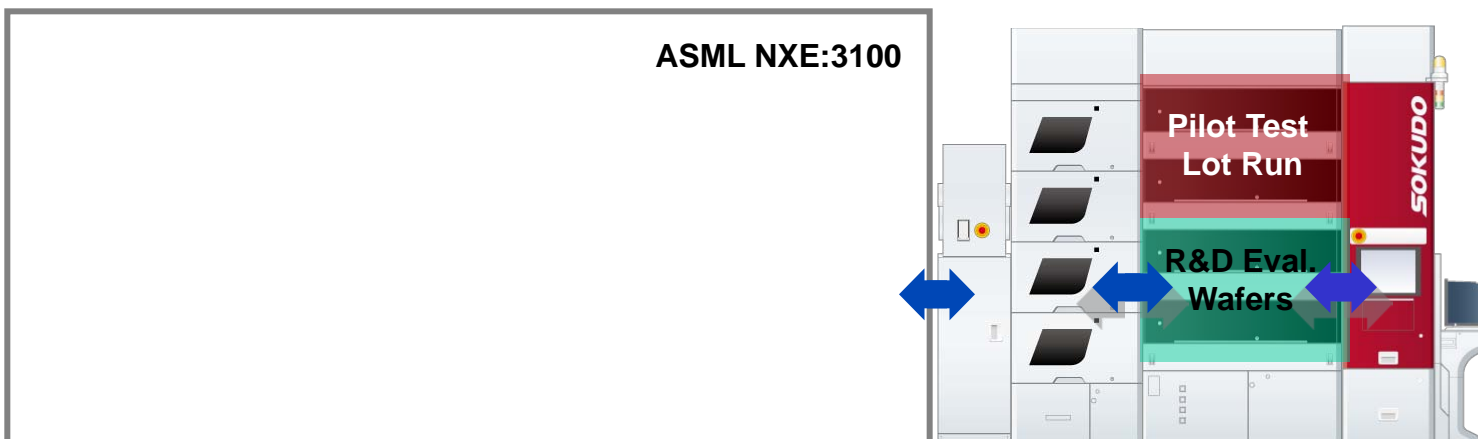
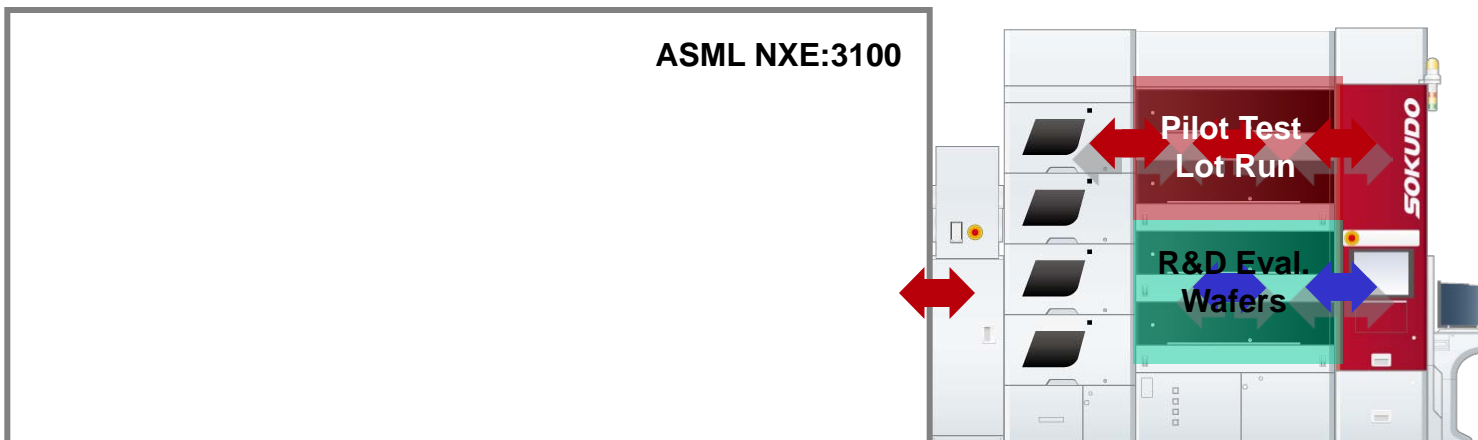
SOKUDO DUO

integration for ASML NXE:3100 (EUV)



- **SOKUDO EUVL Coat/Develop Track Configurations ~120wph**
 - Coat: Underlayer, Resist
 - Develop: TMAH / TBAH developers; various rinse approaches
 - Bake: Biased Hot Plate (QBH) for CDU control / tuning;
“Q” Quick set-temperature change bake between lots

Maximize EUV Lithocell Utilization: Exposure Test Lot Run + R&D Eval. Wafers simultaneously



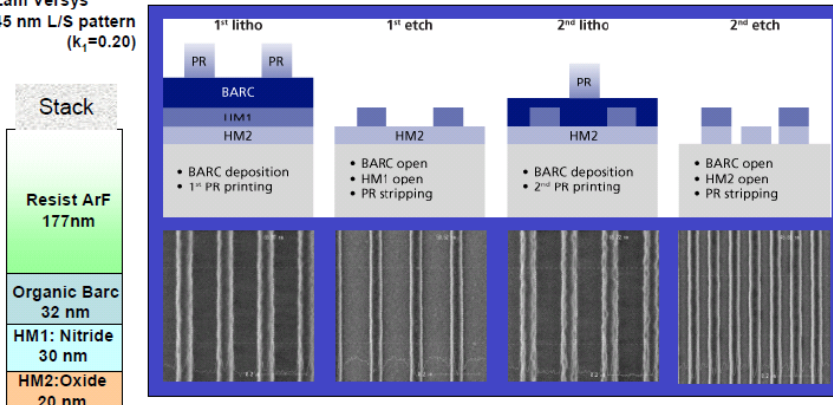
Always keep critical EUV scanner running when available!
KEY for R&D + Pilot Line Productivity!

E-Beam Experience by SOKUDO

- **Advantest F-100 (Japan)**
 - SOKUDO RF3 Coat, Developer in-line with E-Beam
- **Vistec SB3054DW @  Grenoble (France)**
 - SOKUDO RF3 off-line for E-Beam
 - in-line with Nikon NSR-S307

45nm Double Patterning Process

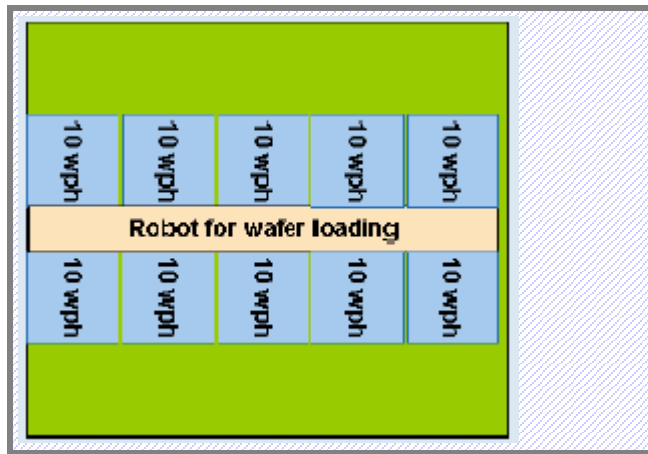
- NSR-S307E 0.85 NA ArF
- Sokudo RF3
- Lam Versys
- 45 nm L/S pattern ($k_1=0.20$)



The End Goal...



E-Beam Coat/Develop Track in-line with MAPPER



MAPPER E-Beam Cluster

Target 100 WPH



SOKUDO DUO Track

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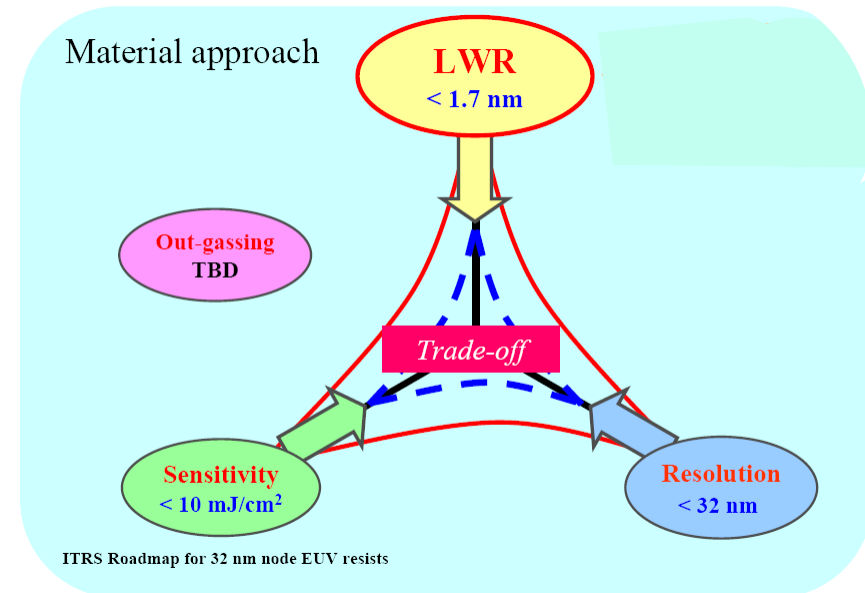
2C = Underlayer
 2C = RESIST
 4D = DEVELOP
 with Backside Scrub
 + E-Beam interface



EUV, E-Beam Common Resist Process Development Focus Points

- **Resist Manufacturers Continuously Reformulating for**
 - Line Width Roughness (LWR)
 - Sensitivity to Dose
 - Resolution 32 nm → 22 nm

- **32 nm → 22 nm CD LWR, Pattern Collapse & Defectivity Track Process Studies:**
 - Develop methods, solutions
 - Rinse methods, solutions



Reference: SPIE 7636-27, February 2010, San Jose, CA USA

SOKUDO EUVL Technical Papers History

SPIE Advanced Lithography 2009

- 7273-111 **Development of EUV resists at Selete**
SELETE (SOKUDO assignee, Koji Kaneyama)
- 7273-115 **EUV resist processing in vacuum**
SELETE, SOKUDO



International Symposium on EUVL 2009



2009 International Symposium on Extreme Ultraviolet Lithography

- Resist II **EUV resist materials and processing at Selete**
SELETE (SOKUDO assignee, Koji Kaneyama)
- Poster 94 **Study of post-develop defect on typical EUV resist**
SOKUDO

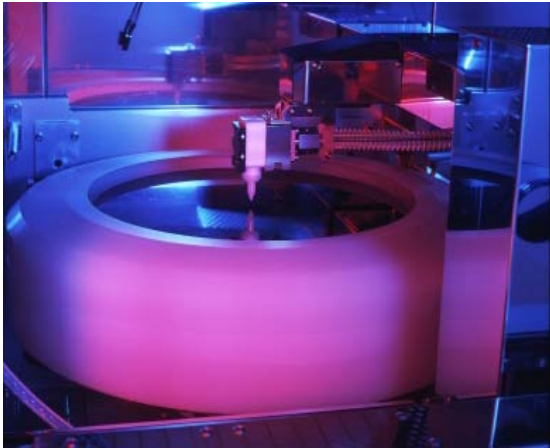
SPIE Advanced Lithography 2010

- 7636-111 **Study of post-develop defect on typical EUV resist**
SOKUDO
- 7636-115 **Alternative resist processes for LWR reduction in EUVL**
SELETE (SOKUDO assignee, Koji Kaneyama)
- 7639-26 **Development of EUV-resists based on various new materials**
SELETE (SOKUDO assignee, Koji Kaneyama)
- 7636-27 **Development of resist material process for hp 2x nm devices using EUV lithography**
SELETE (SOKUDO assignee, Koji Kaneyama)



Coat, Bake & Develop Track Process Knobs

for EUV / E-Beam resist development



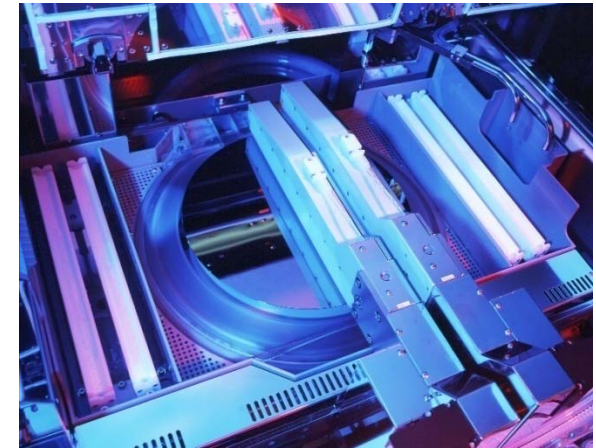
SPIN COAT

- ❖ Dispense Chemistries:
 - ❖ Underlayer +
 - ❖ Photo Resist
- ❖ Thin-film coating recipe
40-60nm thickness



BAKE & CHILL

- ❖ Post-Expose (PEB) for
CD Uniformity control
- ❖ High Temp. (PAB, BARC)



DEVELOP

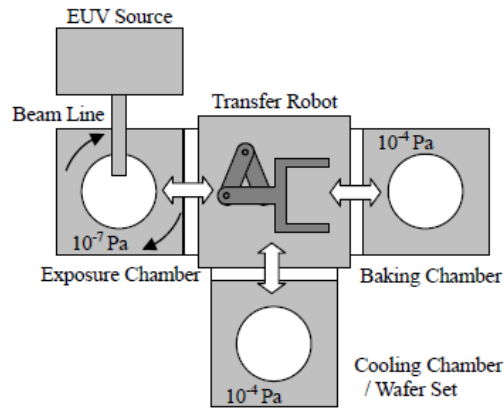
- ❖ Defect Control Approach
 - ❖ Wafer Rinse & Dry
 - ❖ Surfactant Rinse
- ❖ Developer Chemistries:
TMAH, TBAH(?)
Negative Develop(?)

PEB in vacuum vs. atmosphere



Selete

SOKUDO
Custom built Vacuum PEB
“Baking Chamber” &
“Cooling Chamber”



(b) detailed description

EUV Resist Type
MET-2D

Table 3. The lithographic performance of MET-2D with PEB in vacuum and atmosphere

Item	in Vacuum	in Atmosphere
Top-view SEM Image @45nmLS (1:1)		
Cross-section SEM Image		
Esize@45nmLS [mJ/cm ²]	14.1	13.7
Resolution limit [nm]	40	40
LWR [nm]	6.1	7.8

Table 4. The lithographic performance of SSR3 with PEB in vacuum and atmosphere.

EUV Resist Type
SSR3

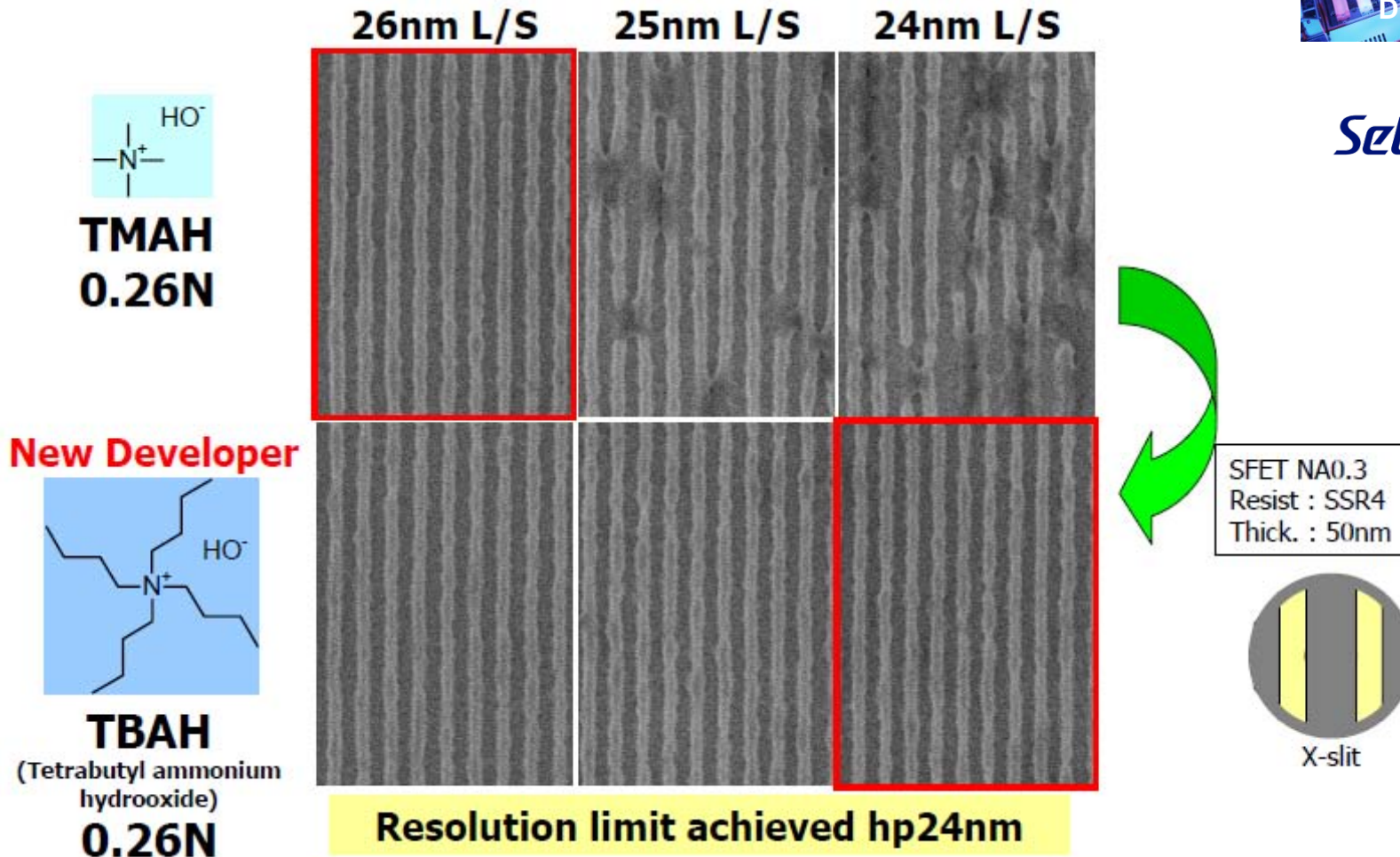
Item	in Vacuum	in Atmosphere
Top-view SEM Image @45nmLS (1:1)		
Cross-section SEM Image		
Esize@45nmLS [mJ/cm ²]	16.0	11.2
Resolution limit [nm]	30	25
LWR [nm]	6.2	4.9

Summary:
Results depend on resist,
PEB in Vacuum may be low value-added

TBAH Developer extends CD capability, reduces pattern collapse



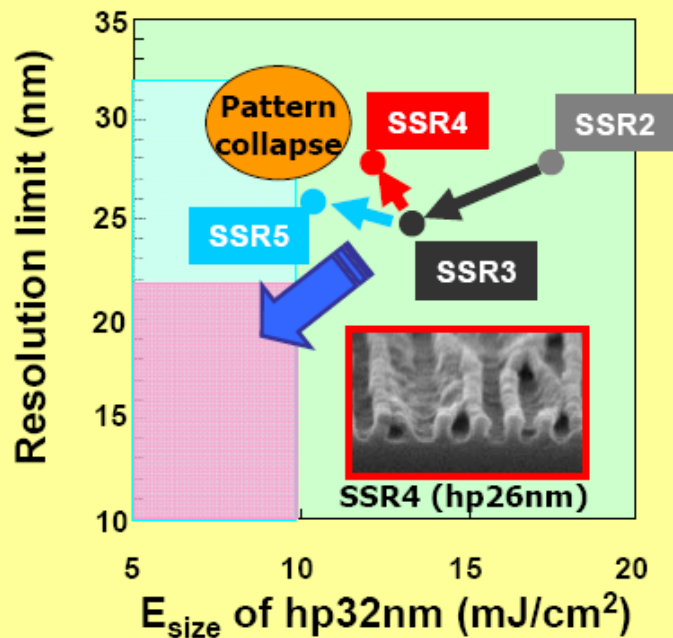
Selete



Reference: EUV resist materials and processing at Selete, K. Matsunaga, et.al.,
International Symposium on EUV Lithography, October 2009, Prague

Pattern Collapse limiting EUV resist resolution

Sensitivity – Resolution



32nm

Targets: Sensitivity (E_{size}): 10mJ/cm²
Short-range LWR : hp x 10%

22nm

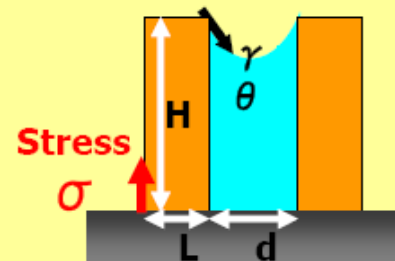
Condition: SFET NA0.3, Illum. Annular (0.7/0.3), Thick: 60nm

Reference: SPIE 7636-27, February 2010, San Jose, CA USA

Model of pattern collapse and improvement by process

Tensile stress

Surface tension



$$\text{Stress } \sigma = \frac{6\gamma \cos \theta}{d} \left(\frac{H}{L} \right)^2$$

H.Namatsu, Appl. Phys. Lett. 66 (20), 1995

- Thinner resist thickness
- Rinse solution
- Additional under layer

Swelling

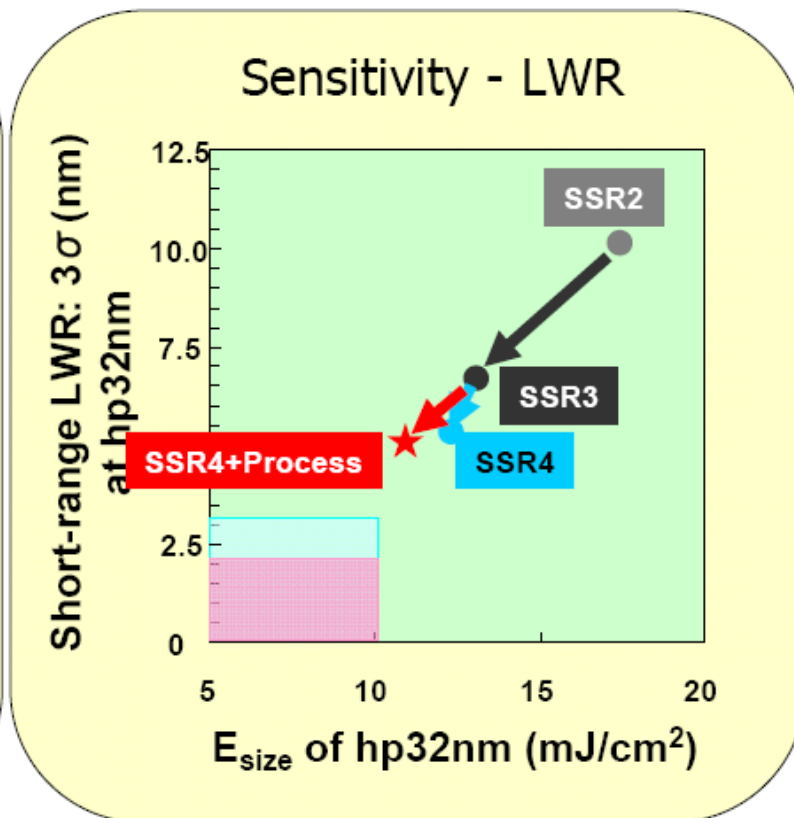
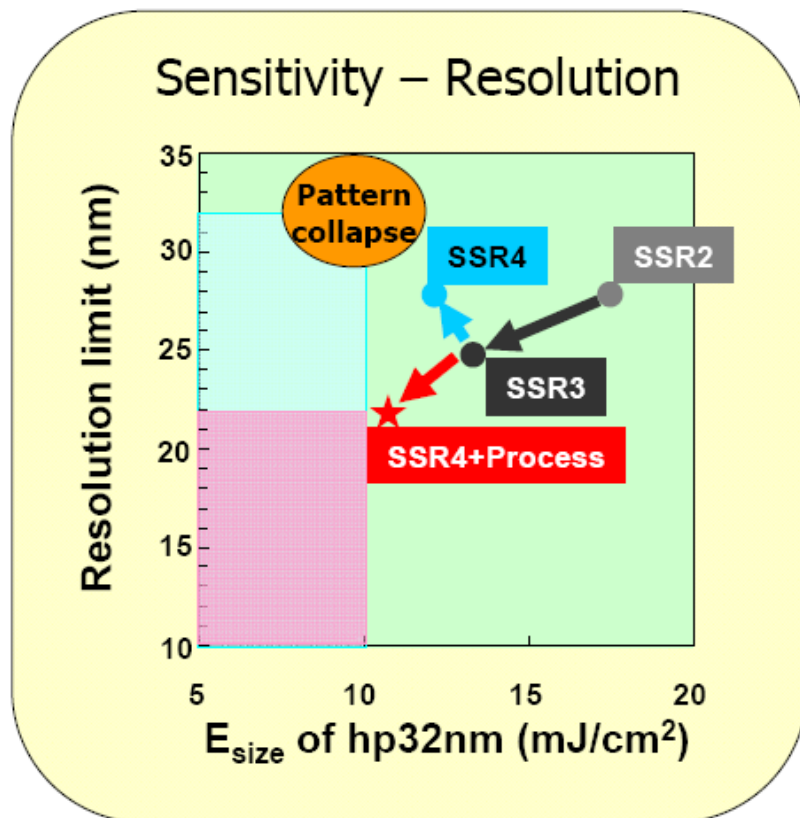


- Developer concentration
- Developer with surfactant
- Bulky developer solution

Selete

SOKUDO DUO

EUV resists improving with each new generation: Resolution, LWR, Sensitivity



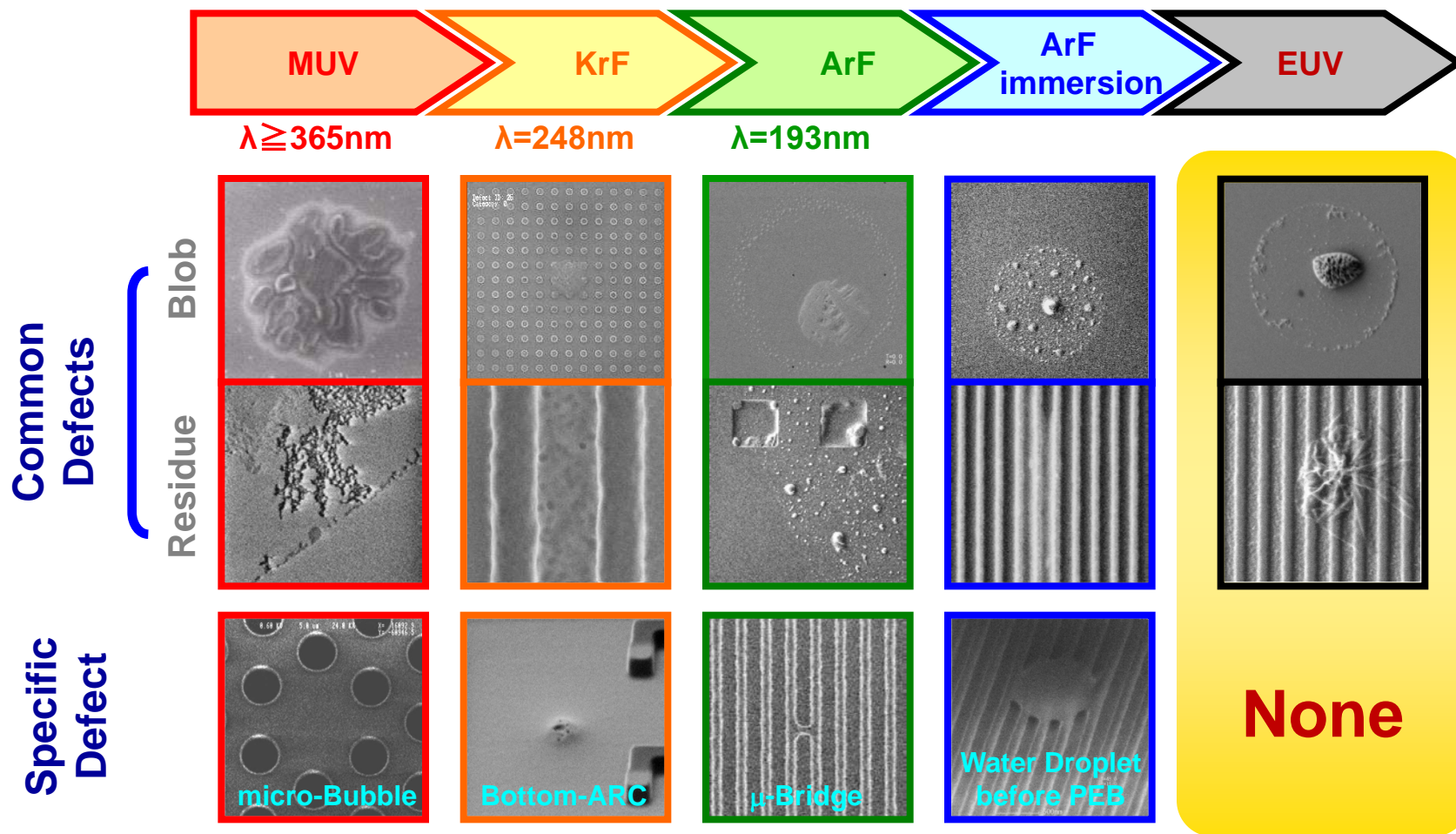
32nm Targets: Sensitivity (E_{size}): $10\text{mJ}/\text{cm}^2$
 22nm Short-range LWR: hp x 10%

SSR# = Selete Standard Resist #



Reference: SPIE 7636-27, February 2010, San Jose, CA USA

Selete

Common / specific defect history; EUV study started



EUV & E-Beam ...

- Although EUV may be leading the march towards 22 nm, E-Beam can close gap with (MAPPER) throughput plans for improvement towards 2012+
- SOKUDO participating in EUV and E-Beam collaborations
 - EUVL consortia resist evaluations and characterization 
 - E-Beam IMAGINE project resist process qualification 
- EUV and E-Beam resists following similar trends and challenges:
 - In parallel transitioning from 32nm → 22 nm process development
 - Both resist systems largely based on reformulating i/KrF generation blends
 - Resist trending to thinner coatings: 40-60 nm target thickness
 - Resolution – LWR – Sensitivity (RLS) all common issues



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