JSR Micro

MATERIALS INNOVATION

JSR

Double Patterning Material Solutions

Sokudo/SEMI Lithography Breakfast Forum - 2008

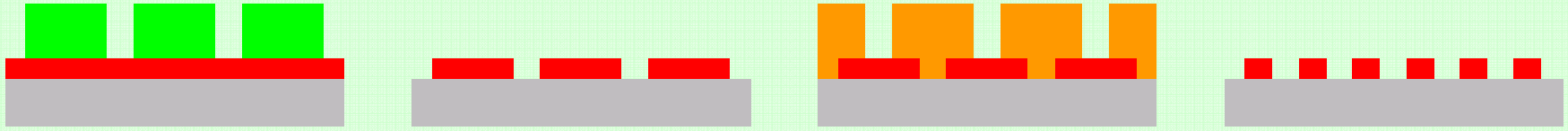
Mark Slezak

Contents

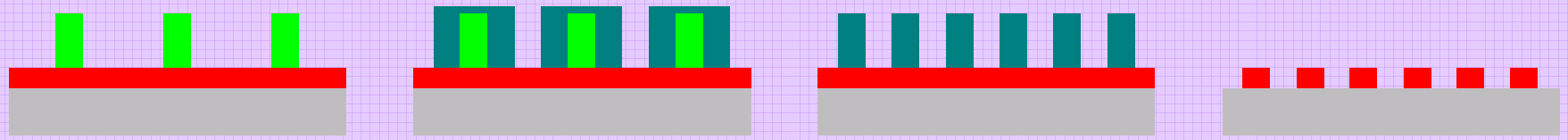
- **Background**:
  - Various Double Patterning Techniques
  - Resist **Freeze** Process
- **Lithography performance of JSR Freeze Process**
  - 32nm LS formation and etching
  - "**Freezing**" process for 2-D logic patterning
  - Contact Hole formation by "**Freezing**" process
- **Summary**

Various Double Patterning Techniques

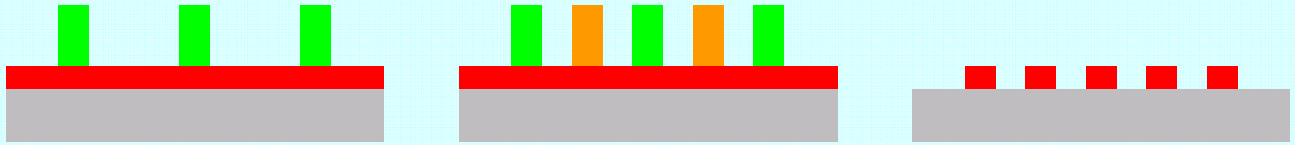
Litho-Etch-Litho-Etch process: Dual-Etch



Side Wall process: Multiple Split and Etch



Litho-Litho-Etch process: Single-Etch

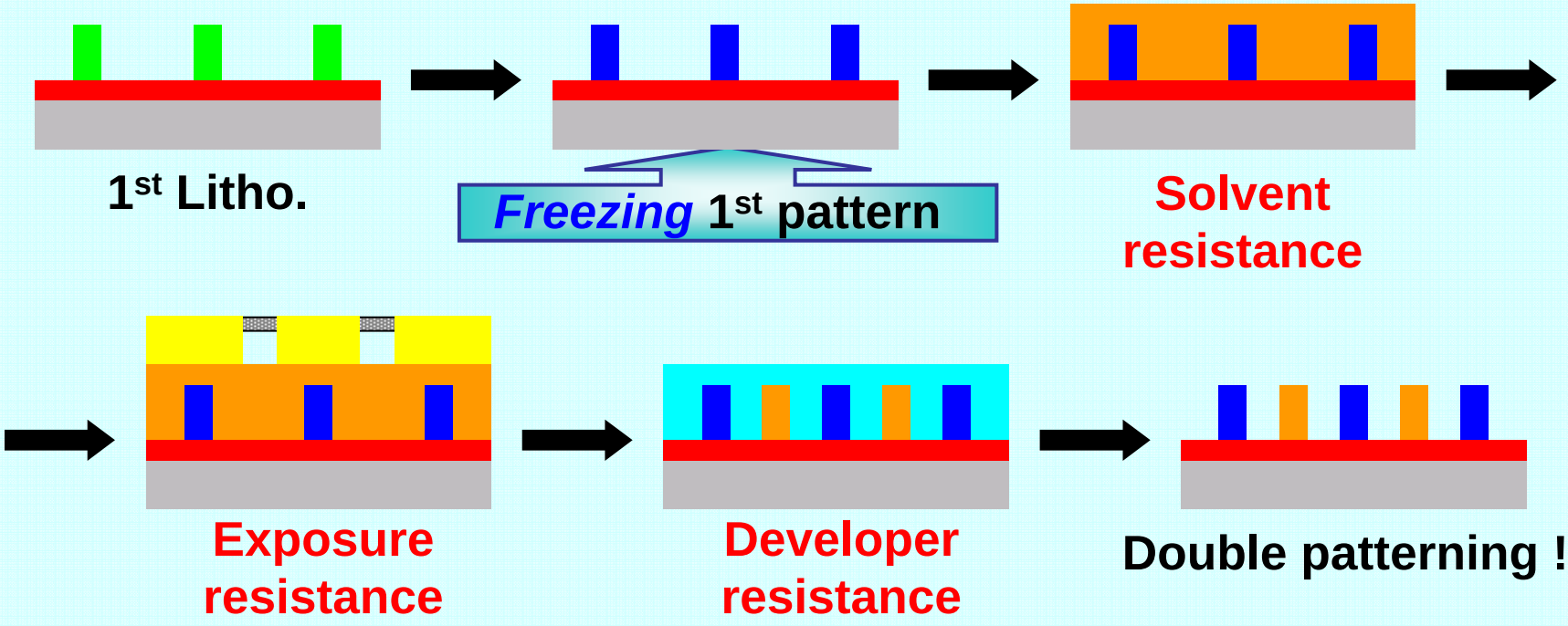


Less Process Steps

*Higher throughput is enabled by **Litho-Litho-Etch** process*

Protection of the 1st layer

Development of "Freezing" process: Litho-Freezing-Litho-Etch



Freezing process provides lot of resistance – *hopefully not to the end user*

Process Flow of "Freezing"

1st litho Patterning | **Freeze Application** | Development

Coat Freeze Material – std. bowl

Bake Freeze Material – std. bake plate (130-160•C)

Develop away "un-used" freezing material – std. developer bowl

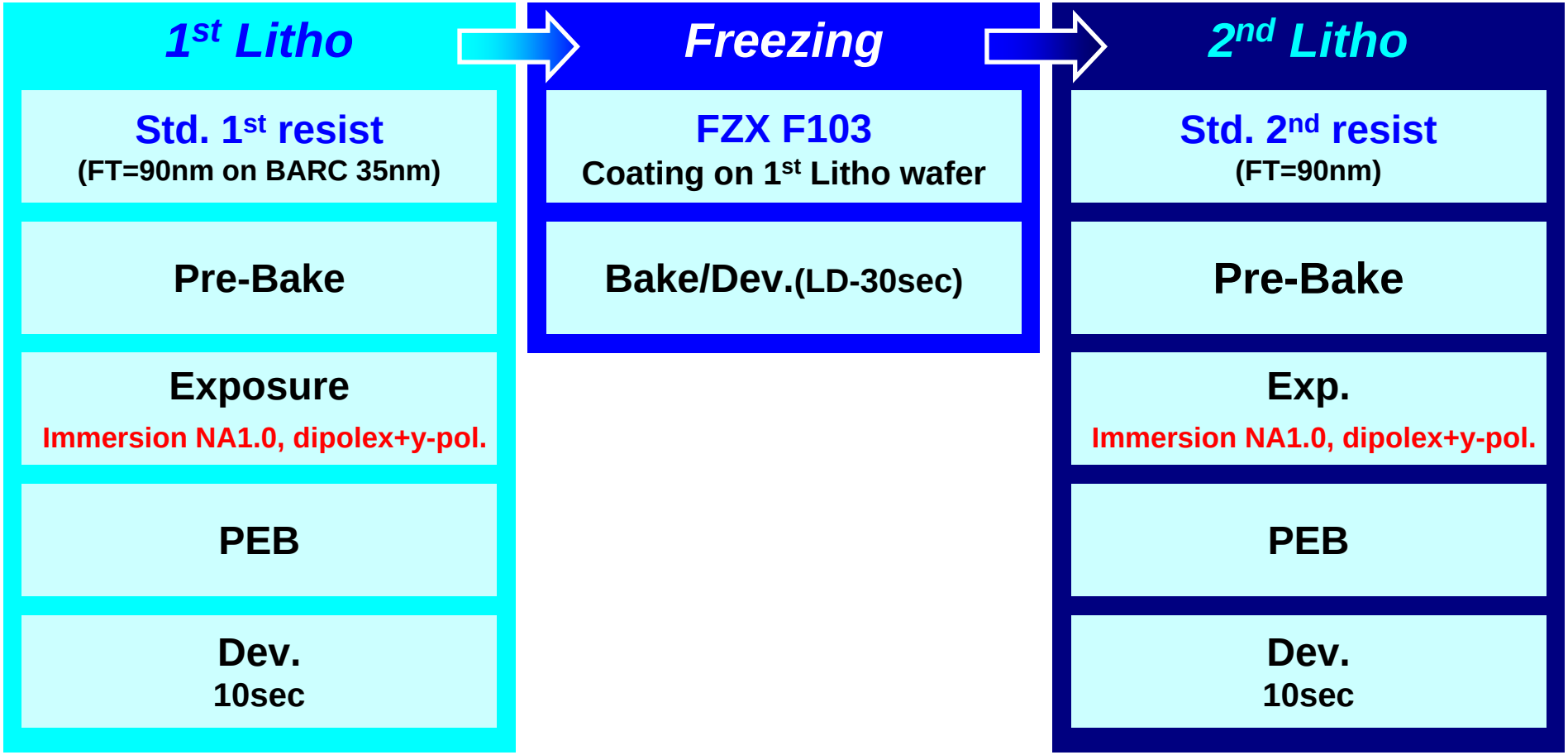
Net result:

- **"Frozen" photoresist that is resistant to further processing**
- **Slightly larger track, however, all conventional components**

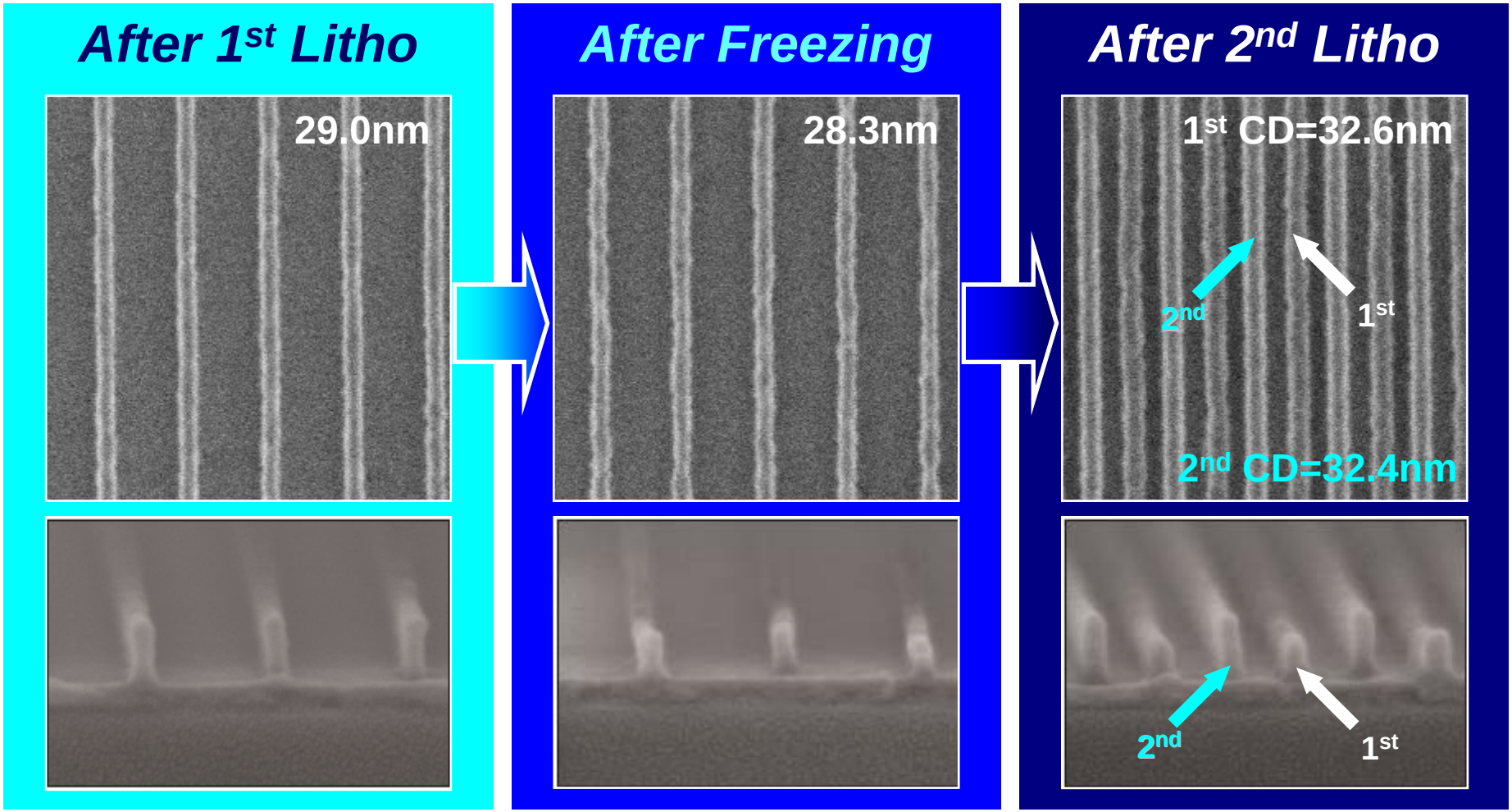
Contents

- **Background**:
  - Various Double Patterning Techniques
  - Resist Freeze Process
- **Lithography performance of JSR Freeze Process**
  - 32nm LS formation and etching
  - “Freezing” process for 2-D logic patterning
  - Contact Hole formation by “Freezing” process
- **Summary**

Experimental Condition

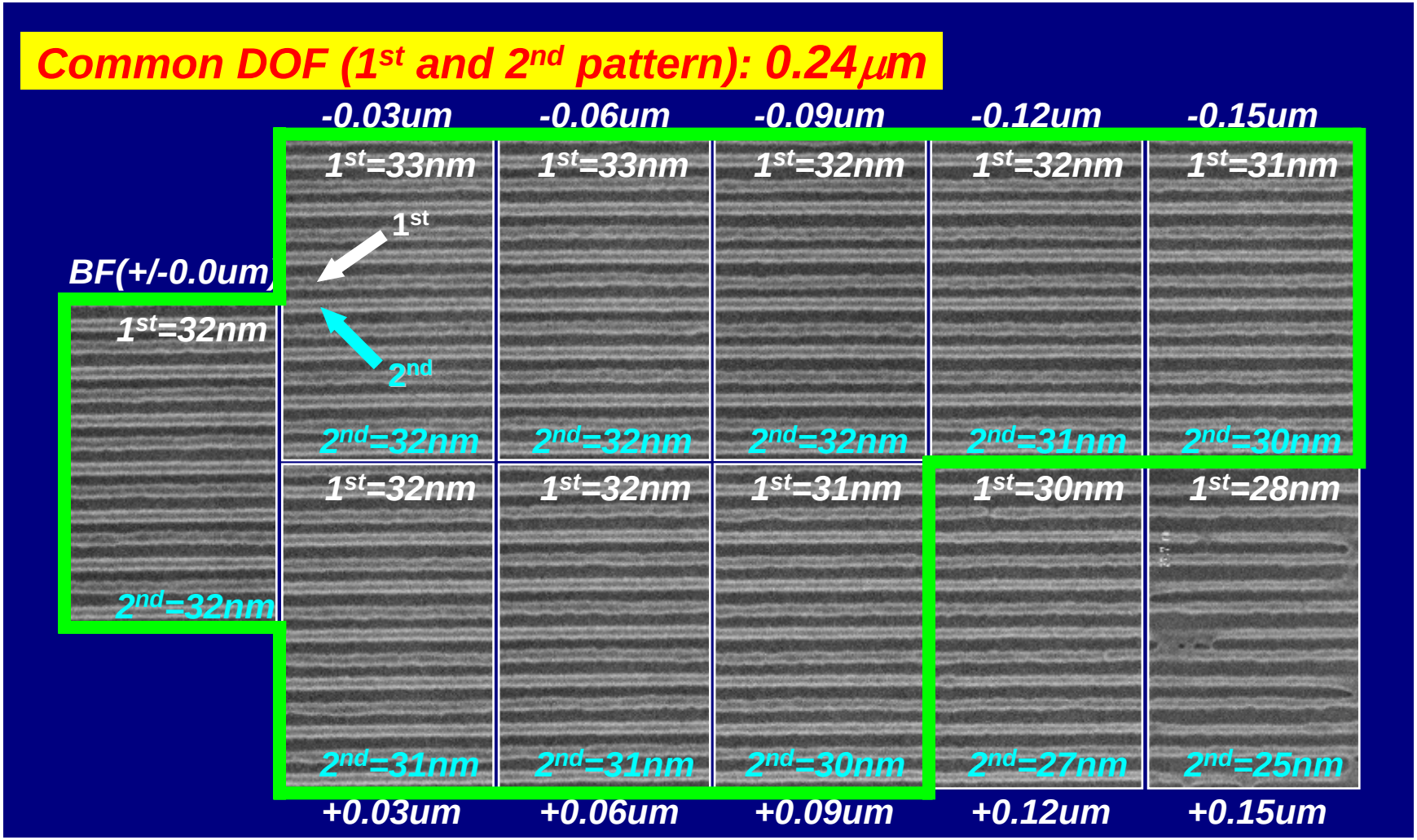


Formation of 32nmLS Pattern



➢ ***Formation of 32nmLS double patterning***

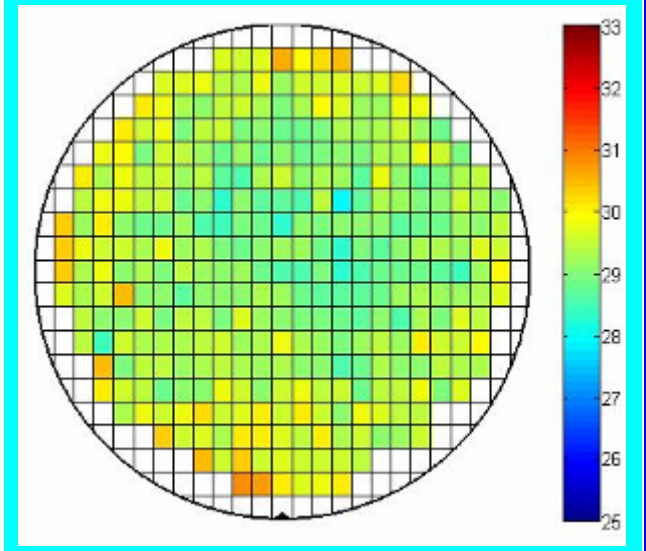
Common DOF after 2nd Litho



- After 2nd litho, 240nm common DOF in both 1st and 2nd litho patterns of 32nmLS was obtained

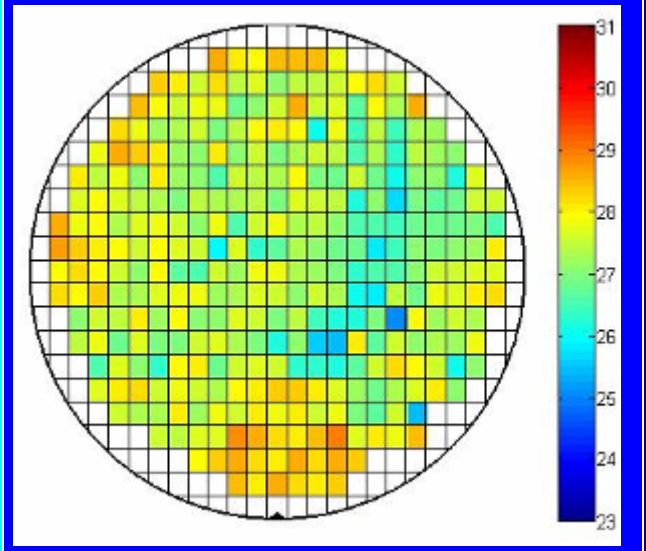
CD Uniformity of 32nmLS Pattern

After 1st Litho



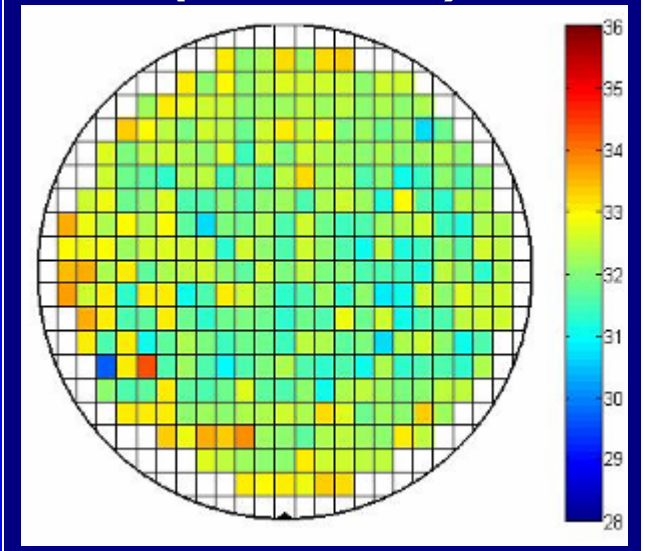
average	29.3nm
3σ	1.36nm
max	30.8nm
min	28.0nm
range	2.8

After Freezing



average	27.4nm
3σ	1.96nm
max	28.9nm
min	25.1nm
range	3.8

After 2nd Litho (1st Pattern)



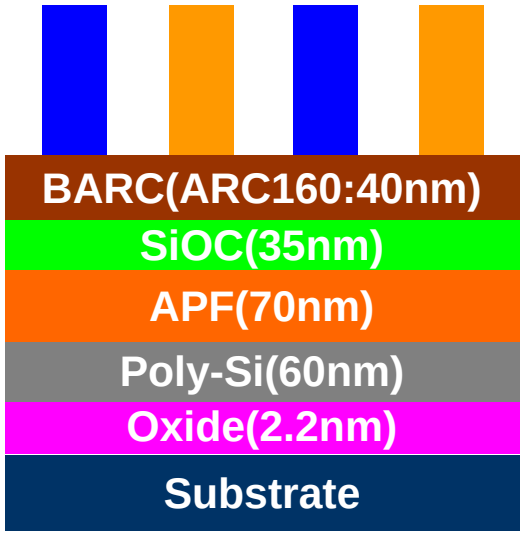
average	32.2nm
3σ	1.86nm
max	34.3nm
min	29.7nm
range	4.6

➢ ***CD uniformity of 1st litho pattern was kept within 2nm through double patterning step with freezing process***

Etching Experiment for "Freezing"

➢Materials

- 1st resist: **JSR standard resist** (FT=120nm(40nmL80nmP)/90nm(32nmL64nmP))
- Freezing materials: **FZX F103**
- 2nd resist: **JSR standard resist** (FT=90nm)



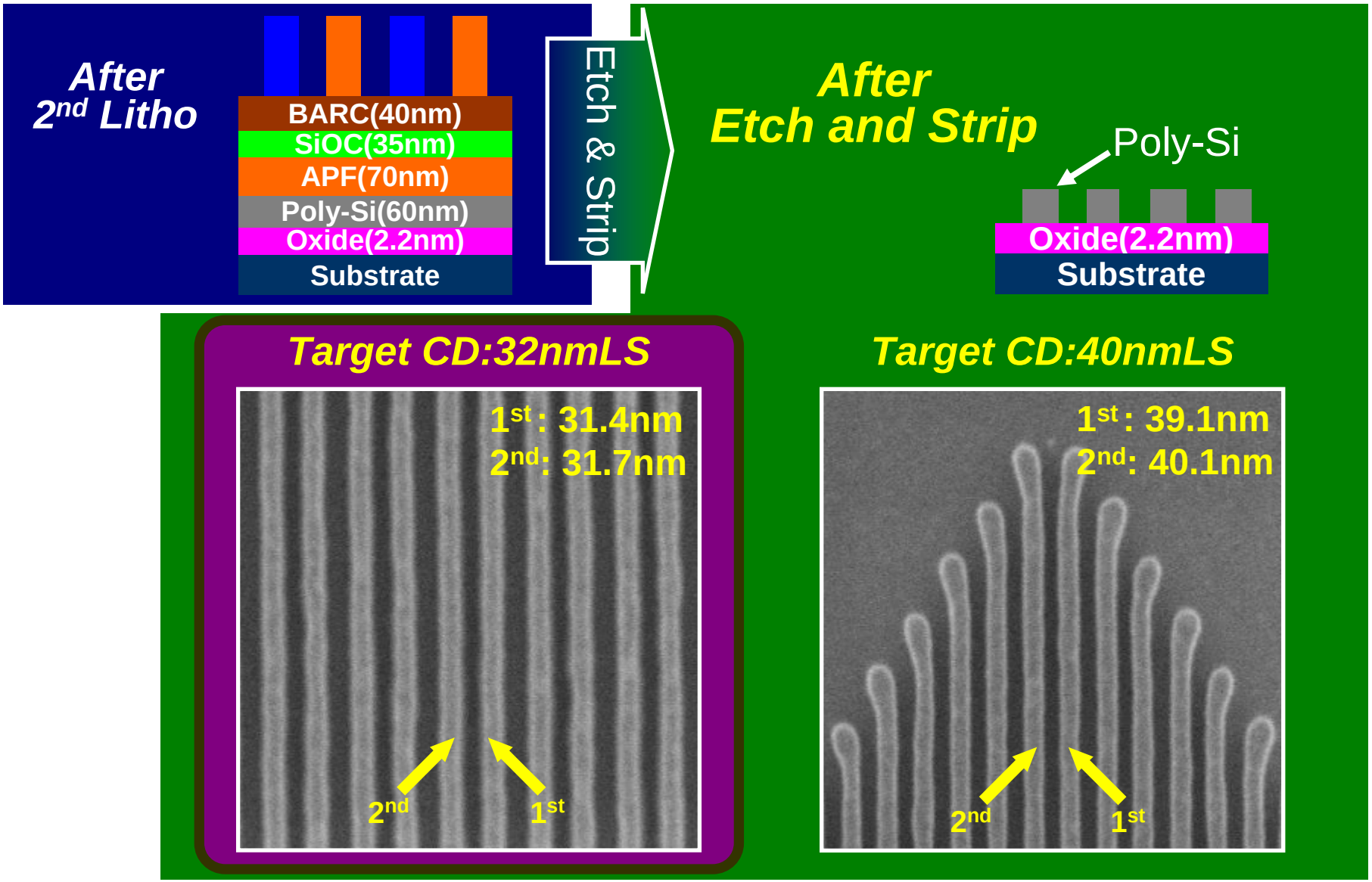
➢Organic/Inorganic stack

- BARC : 40nm / SiOC:35nm / APF : 70nm / Poly : 50nm / Oxide : 2.2nm

➢Target CD & Exposure/Illumination condition

- ***40nmLS***: NA=1.2, Annular(0.8/0.5) + xy-pol.
- ***32nmLS***: NA=1.0, Dipole40 + pol.

Etching Results of 40&32nm LS Pattern

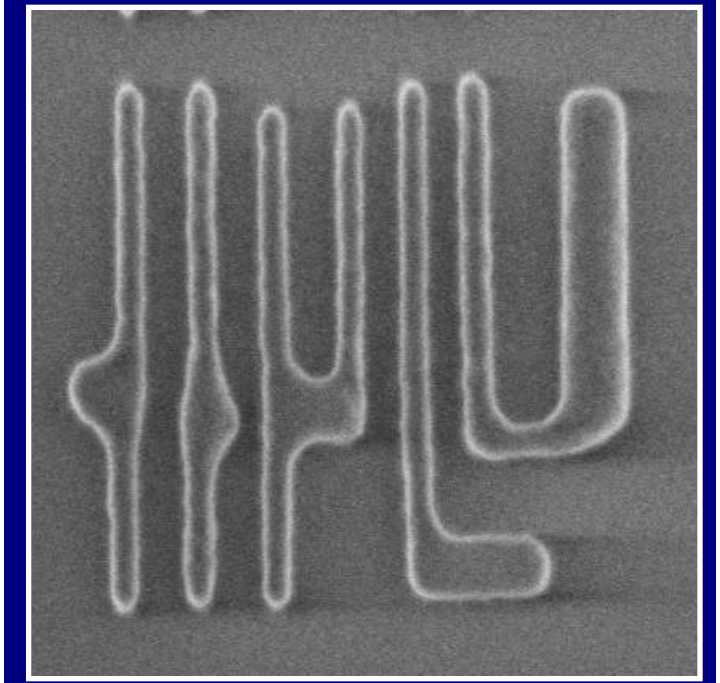


Contents

- **Background**:
  - Various Double Patterning Techniques
  - Resist Freeze Process
- **Lithography performance of JSR Freeze Process**
  - 32nm LS formation and etching
  - “Freezing” process for 2-D logic patterning
  - Contact Hole formation by “Freezing” process
- **Summary**

"Freezing" Process for 2D Logic Patterns

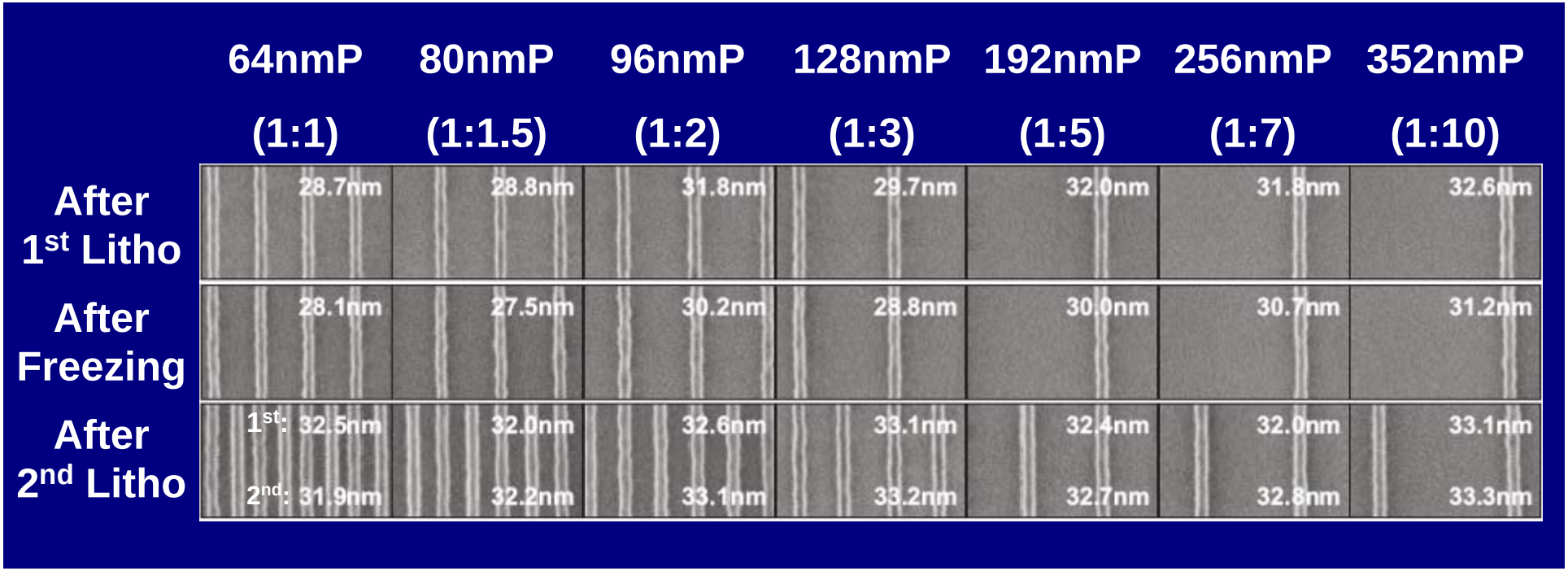
After 2nd Litho
40nm Logic Pattern
CD~45nm



- **Can we handle 2D logic patterning with "Freezing" process?**

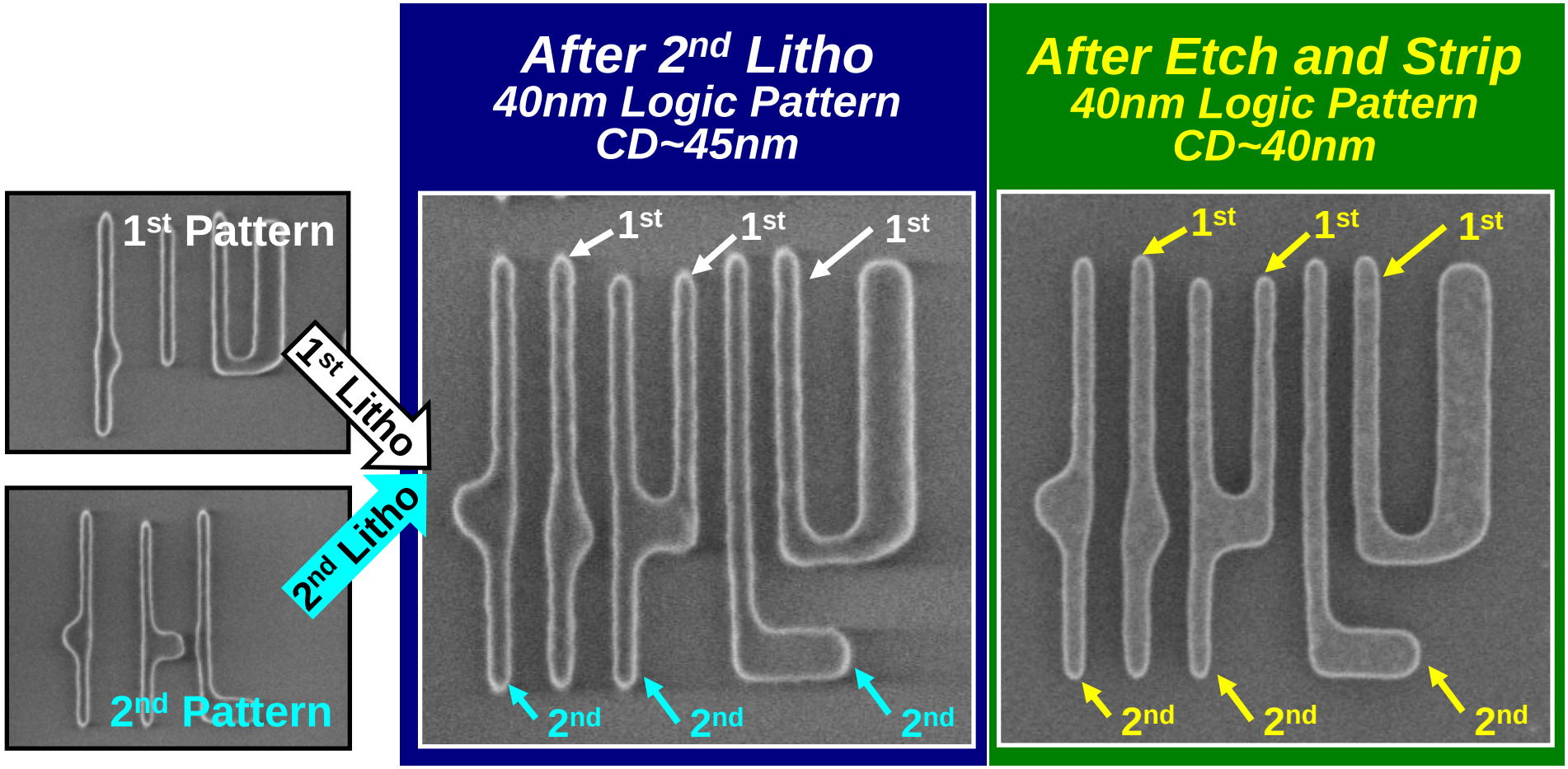
CD Control through "Freezing" Process

✓ ***For complex 2D application, the pitch dependency of freezing process on 1st pattern CD variation is important.***



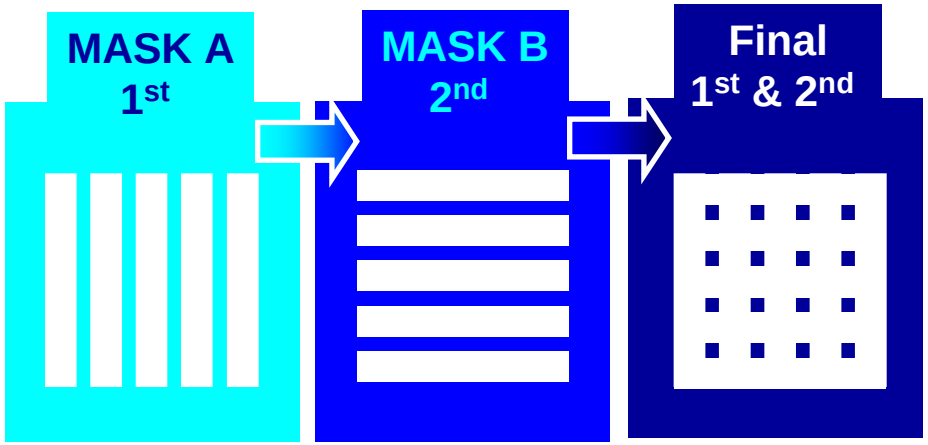
➢ ***Freezing technique works well for 32nm various pitch patterns.***

Etching Results of 2D Logic Pattern



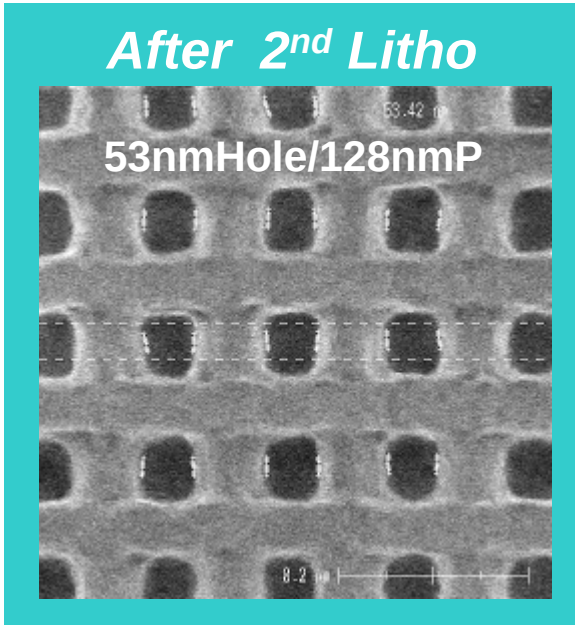
- ***Freezing technique is also available for complex 2D pattern.***
- ***Configuration of litho pattern was kept after etching.***

Cross-Lines CH Double Patterning



- **Hole feature can be generated by using x/y-cross lines method with freezing process.**

- **Exposure/Illumination** NA=1.2, Ann(0.8/0.5)+xy-pol.



Summary

- ✓ *Resist "Freezing" processes have been developed for Litho-Litho-Etch double patterning applications*
- ✓ *32nm half-pitch, 2-D logic patterns, and even contact hole patterns have been imaged using the resist freeze process*
- ✓ *Etch work through our partners at IMEC show excellent image transfer using materials that were processed with the freeze materials*
- ✓ *Resist Freeze is an elegant way of reducing process complexity and cost.*